

AMD AM4

B550

MS-7C56-10 C

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35	Audio DePop	66	LED - JRGB1_JRANBOW1/2		

AMD
Summit Ridge
Raven Ridge
Pinnacle Ridge
Matisse Ridge
Renoir Ridge
Vermeer Ridge
Zen2

105W

SOCKET 1331

Promontory

B550
(PROM19.C)

P_HUB
P [3:0]

Rear I/O
HDMI
DP
DP/HDMI1

SPI Flash ROM
256M bit 1.8V
SPI1

PCIe x16 Slot
PCIe_E1

M.2
PCIe Mode Only
M2_2

PCIe x4 Slot
PCIe_E3

PCIe x1 Slot
PCIe_E4

PCIe x1 Slot
PCIe_E2

LAN - RTL8111H
LAN_USB1

SATA 3.0 x1
SATA5

SATA 3.0 x1
SATA6

SATA 3.0 x2
SATA1_2

SATA 3.0 x2
SATA3_4

CHA PC4-3200
CHB PC4-3200
DDR4 UDIMM x2
DDR4 UDIMM x2

PCIe Gen4 x4 P_GPP[0:3]
M.2
PCIe Gen4 x4
PCIe/SATA Mode
M2_1

LPC
SIO
NUVOTON
NCT6687D-R
PS2 I/F
Rear I/O
PS2 Combo
PS2_USB1

USB 3.2 x2 USB_SS[1:3]
USB 2.0 x2 USB_HSD[1:3]
RE-DRIVER
PI3EQX1004
USB 3.2 Gen2 x2
Rear TYPE-A+C
USB 3.2 x2
USB2+USB3

USB 3.2 x2 USB_SS[0/2]
USB 2.0 x2 USB_HSD[0/2]
USB 3.2 Gen1 x2
Rear TYPE-A
USB 3.2 x2
LAN_USB1

USB 3.2 x1 USB_SSP[0]
USB 2.0 x1 USB_HSD[0]
RE-DRIVER
ASM1464
USB 3.2 Gen1 x1
Front Type-C
USB 3.2 x1
JUSB4

USB 3.2 Gen1 x2 USB_SS[0:1]
USB 2.0 x2 USB_HSD[2:3]
Front Type-A
USB 3.2 x2
JUSB3

USB 2.0 x2 USB_HSD[4:5]
Rear I/O
PS2 Combo
PS2_USB1

USB 2.0 x1 USB_HSD[1]
GL850G
Front I/O
USB 2.0 x2
JUSB1

Front I/O
USB 2.0 x2
JUSB2

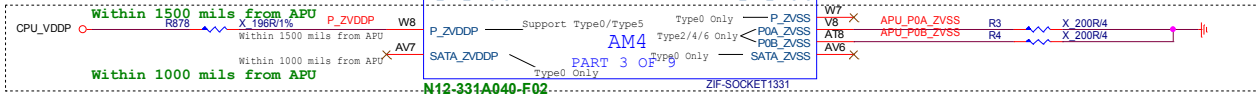
USB 2.0 x1 USB_HSD[6]
MCU
NUC126NE4AE
U63

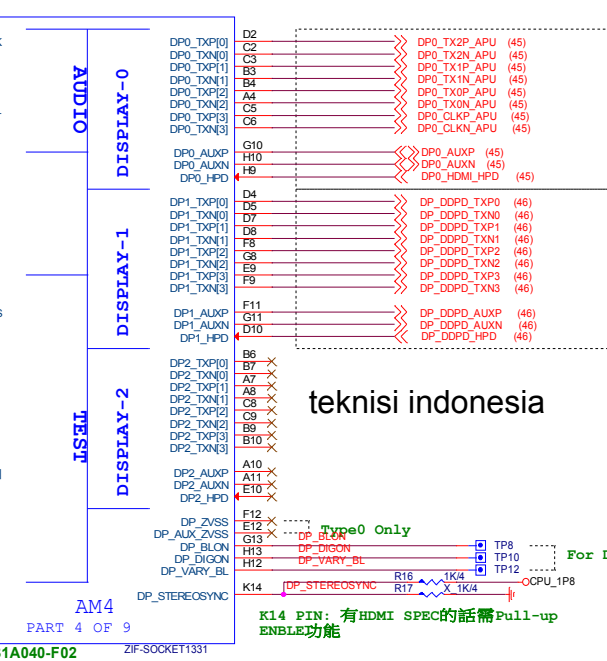
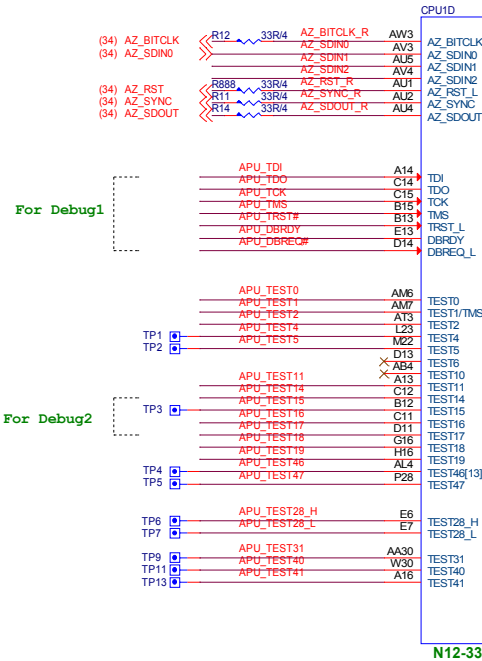
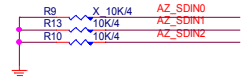
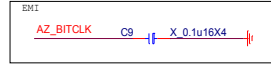
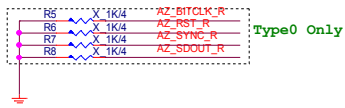
USB 2.0 x2 USB_HSD[8/9]
Rear TYPE-A
USB 2.0 x2
USB1

SATA 0 supported M.2
Not supported PCIE on TYPE 0

TYPE	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

Only supported on TYPE 2/4





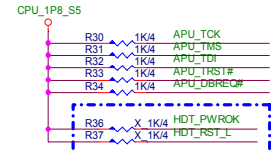
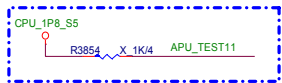
For HDMI

For DP

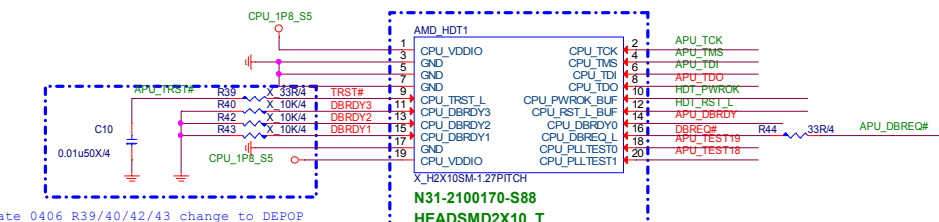
Not supported on TYPE 2/4

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update 0406 add pull up CPU_1P8_S5 to APU_TEST11

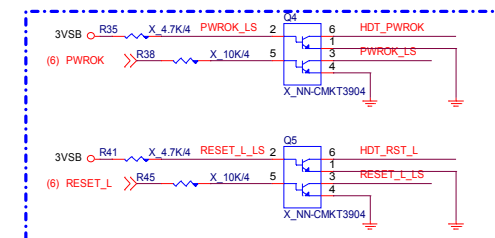


update 0406 R36/37 change to DEPOP



update 0406 R39/40/42/43 change to DEPOP

update 0406 AMD_HDT1 change to DEPOP



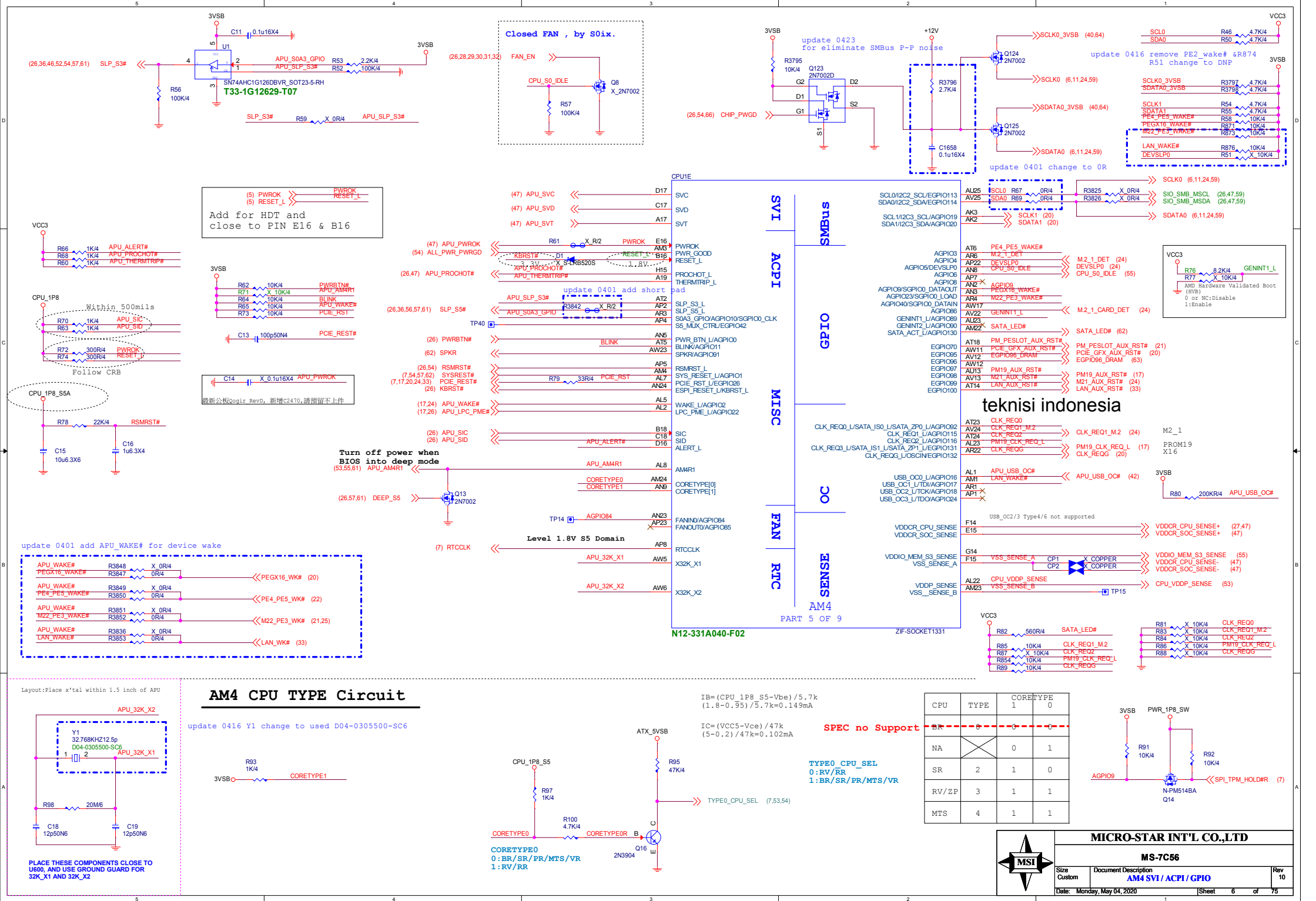
update 0406 R35/38/41/15 and Q4/5 change to DEPOP

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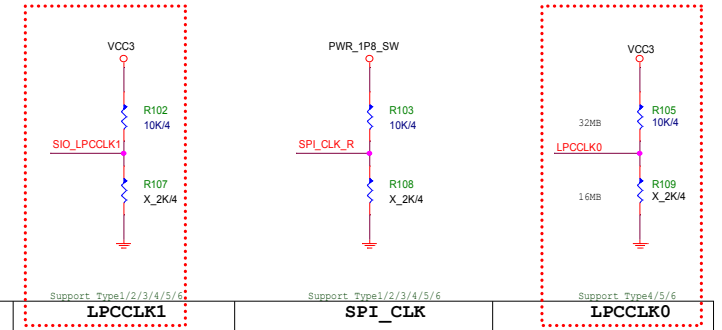
MS-7C56

Size Custom Document Description AM4 Display / Audio Rev 10

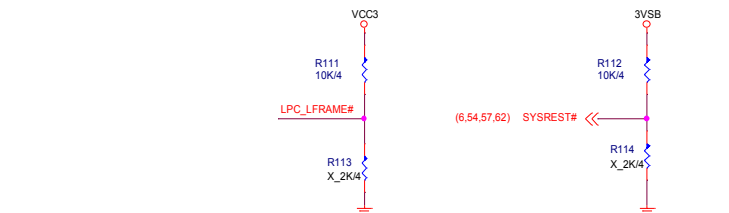
Date: Monday, May 04, 2020 Sheet 5 of 75



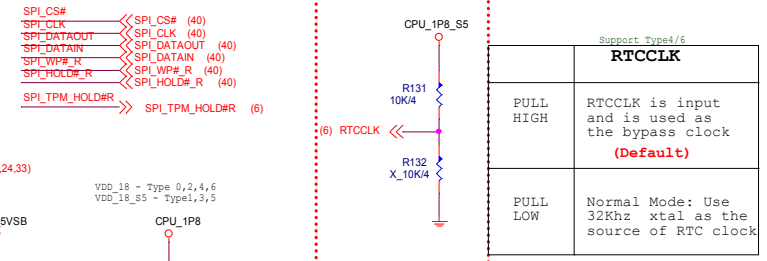
Strapping Options



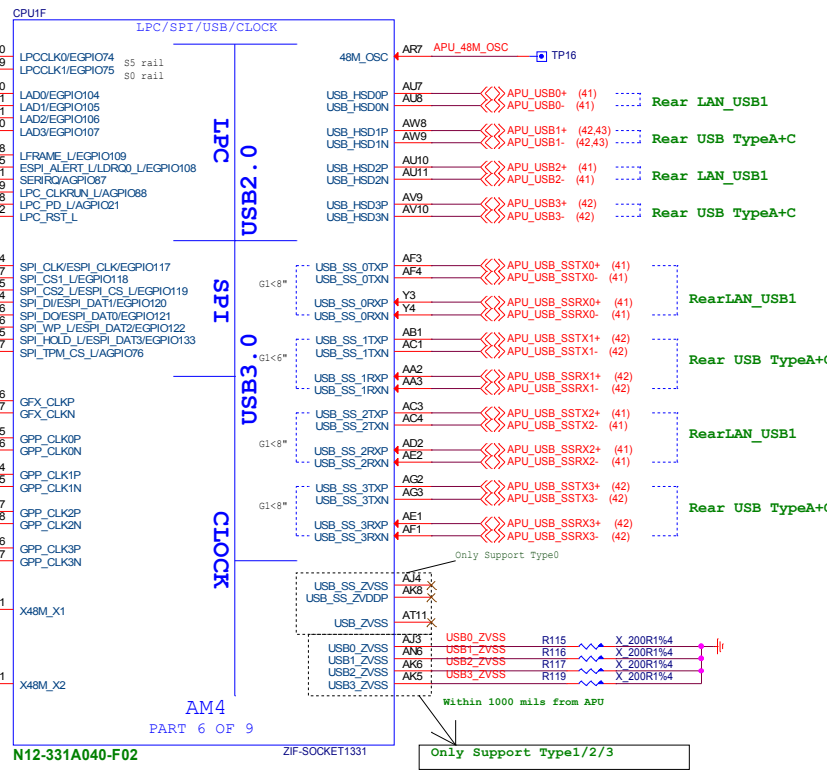
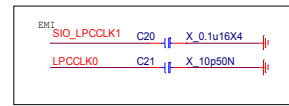
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

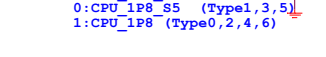
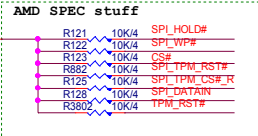
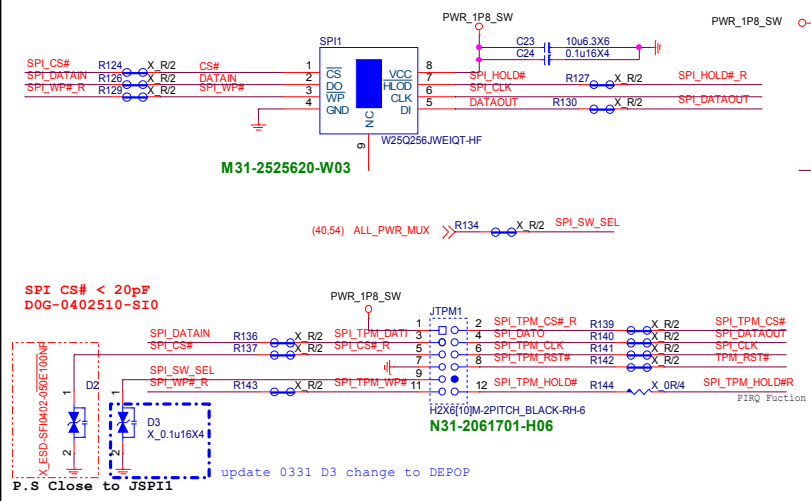
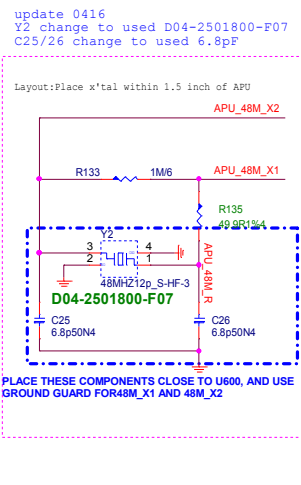


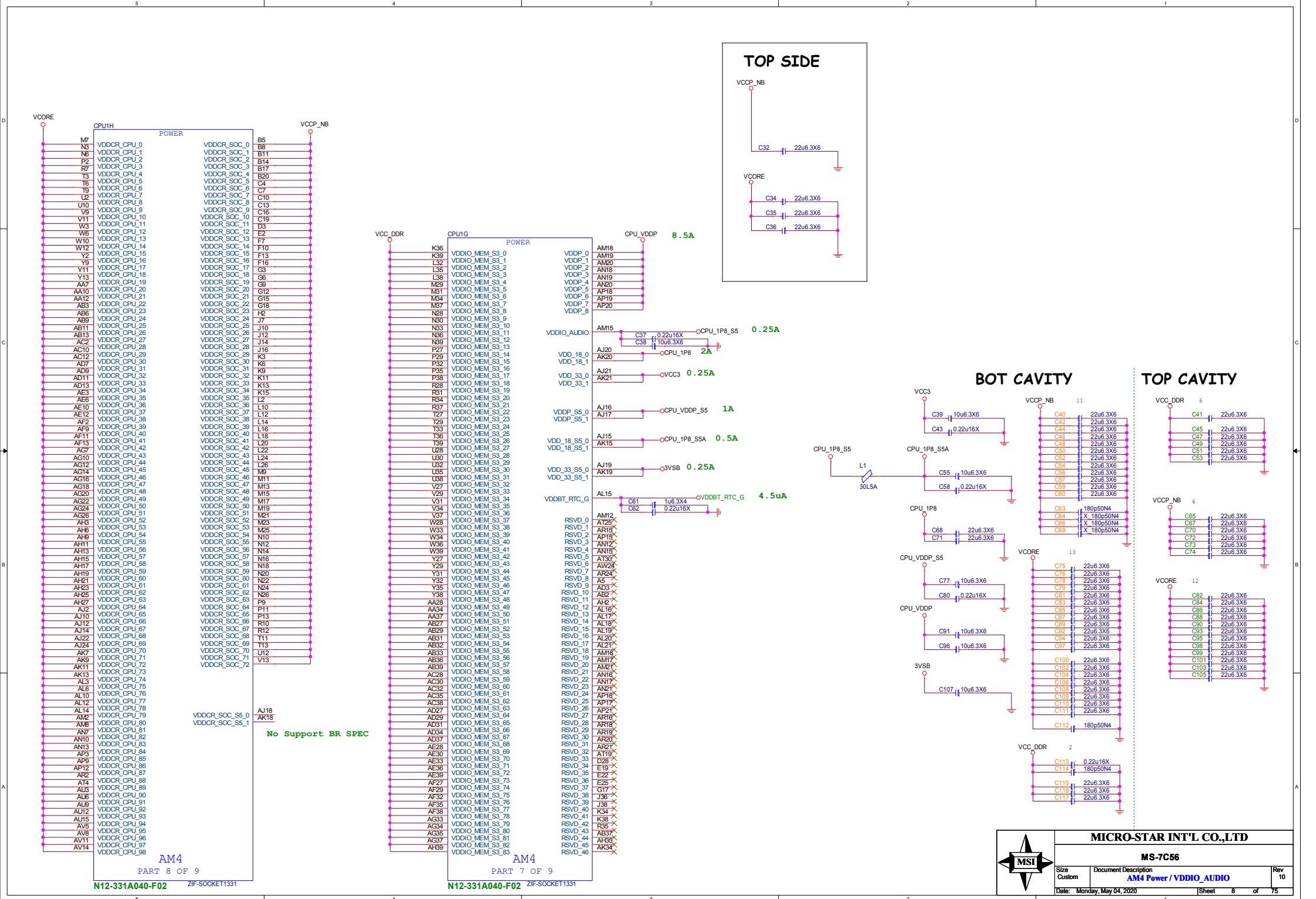
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MS-7C56		
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AM4 LPC/SPI/USB/CLK/STRAP		
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SPI ROM (1.8V)

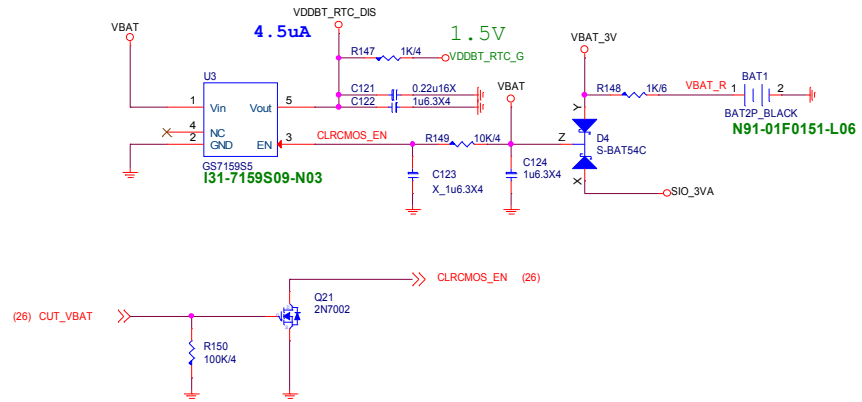




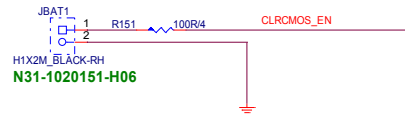
GND

AM4
PART 9 OF 9

RTC & Clear CMOS Circuit



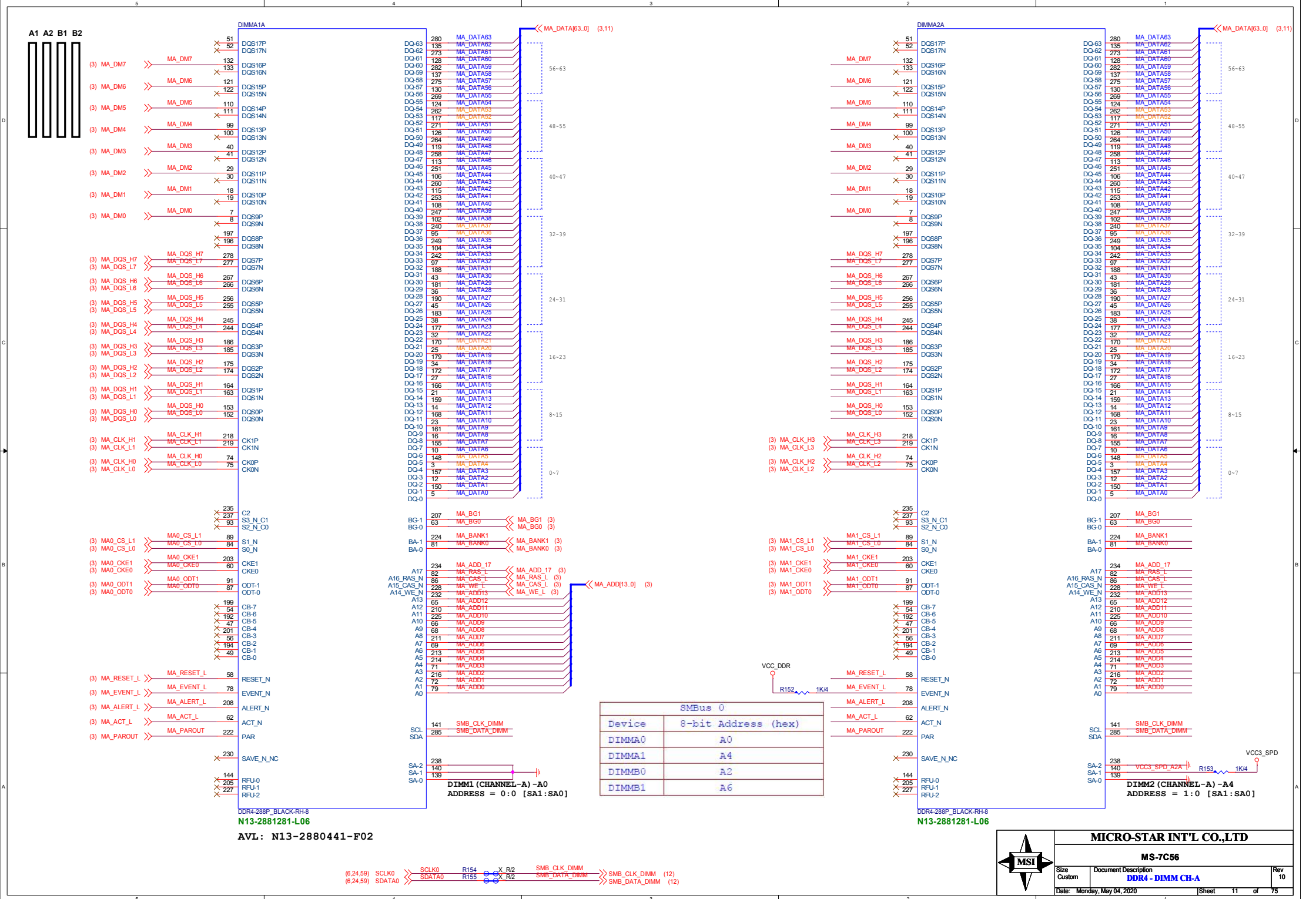
Clear CMOS button

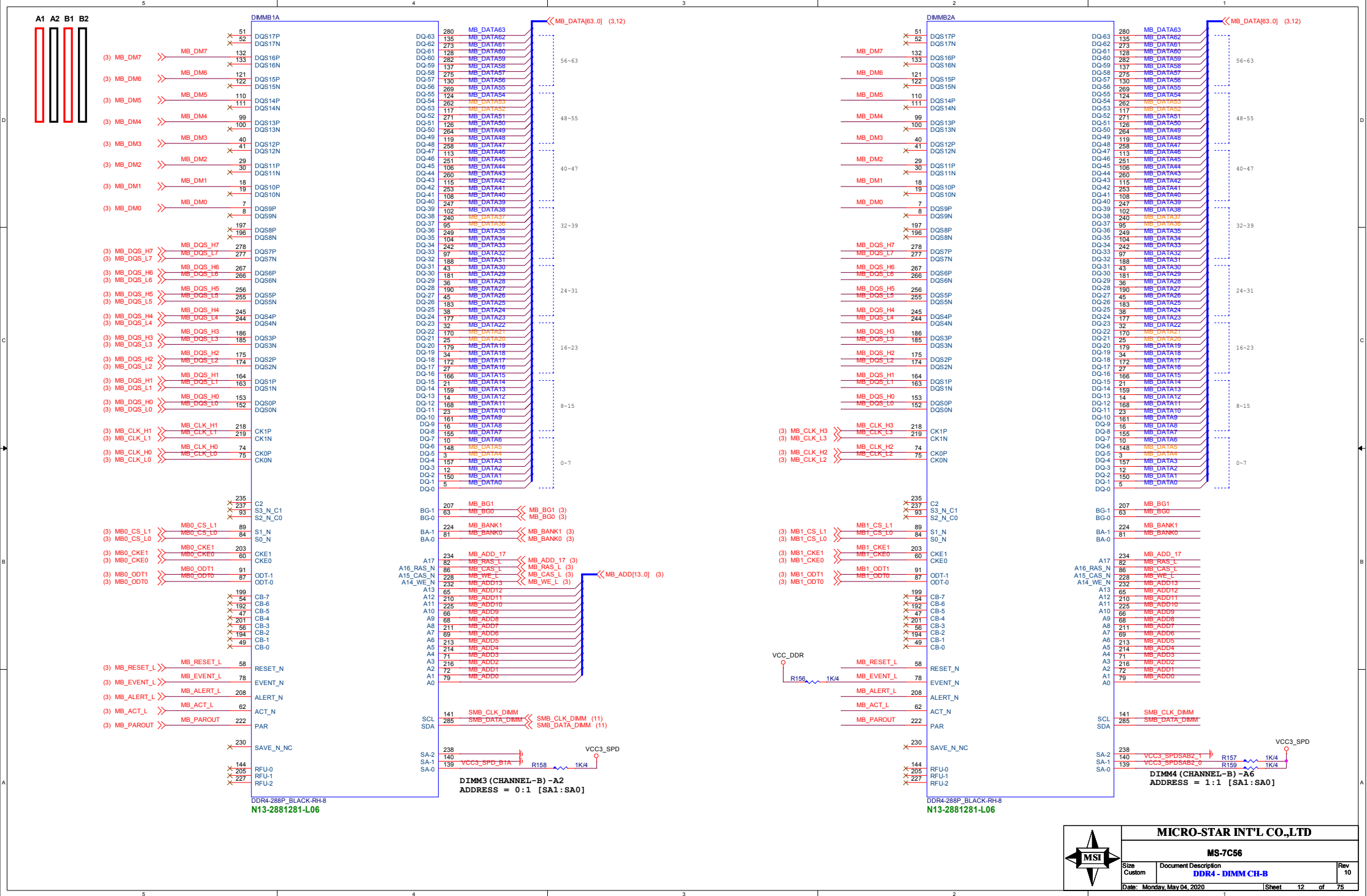


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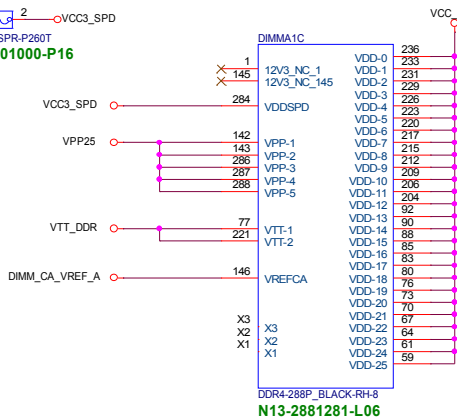


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MS-7C56		
Size	Document Description	Rev
Custom	DIMM4 - DIMM CH-B	10
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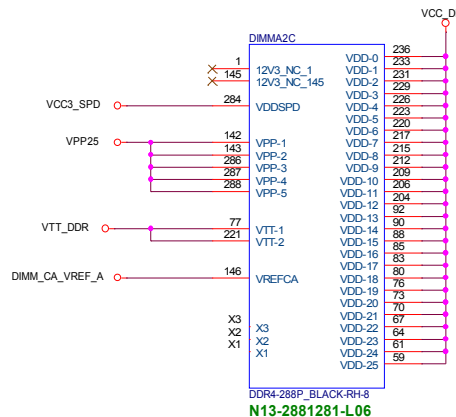
av1:D08-0301100-B07

VCC3 1 F1 2 VCC3_SPD

F-SPR-P260T
D08-0301000-P16

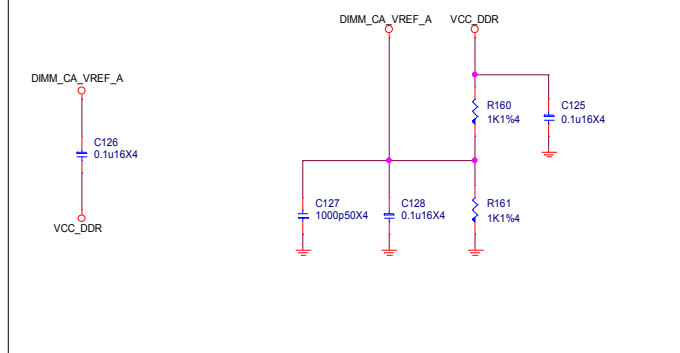


DIMM SLOT PN BY SPEC

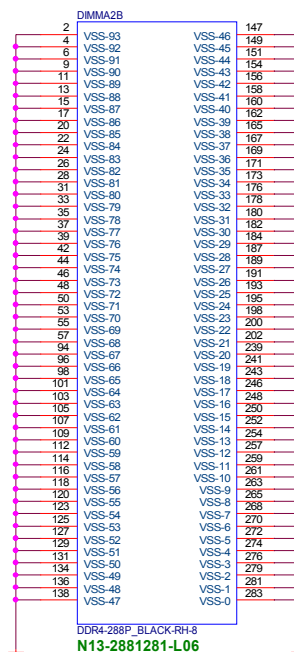
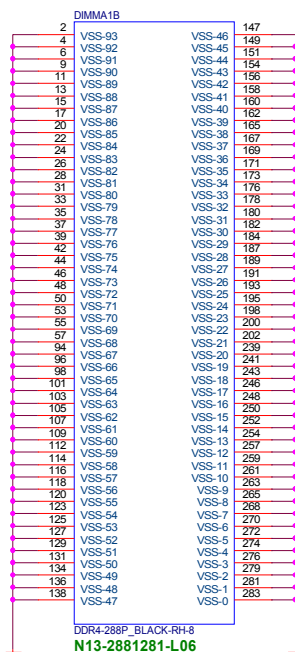
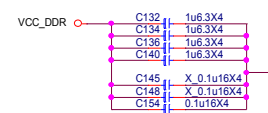
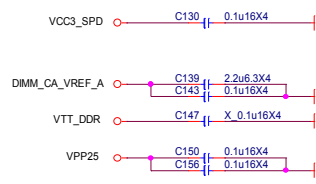
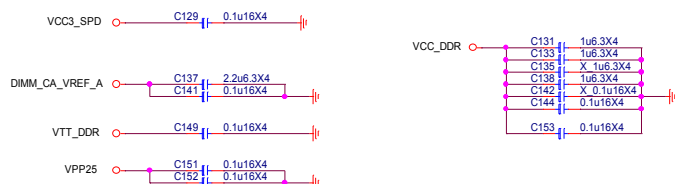


DDR VREF

(place resistors close to DIMMs)



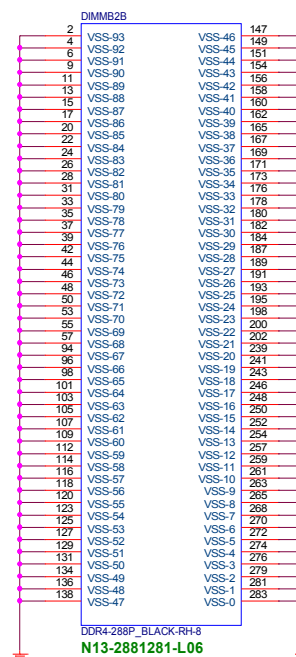
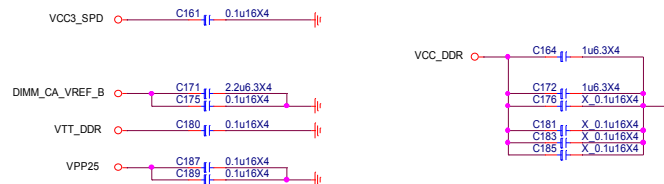
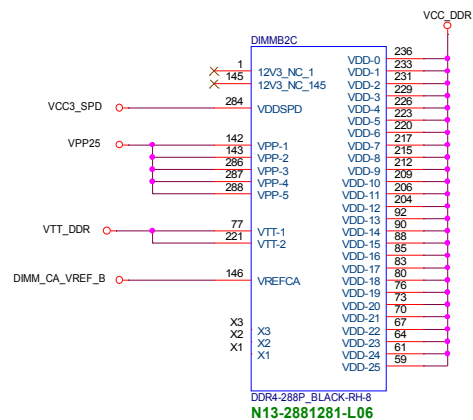
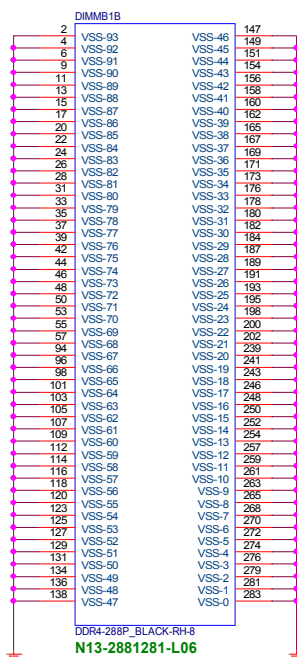
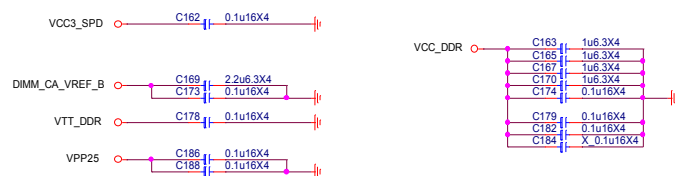
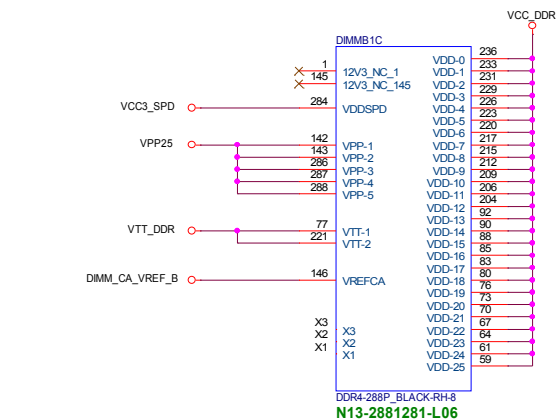
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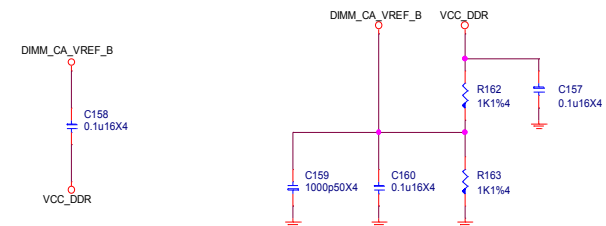
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Custom	DDR4 - POWER/GND-1	10
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DDR VREF

(place resistors close to DIMMs)



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Size Custom	Document Description DDR4 - POWER/GND-2	Rev 10	
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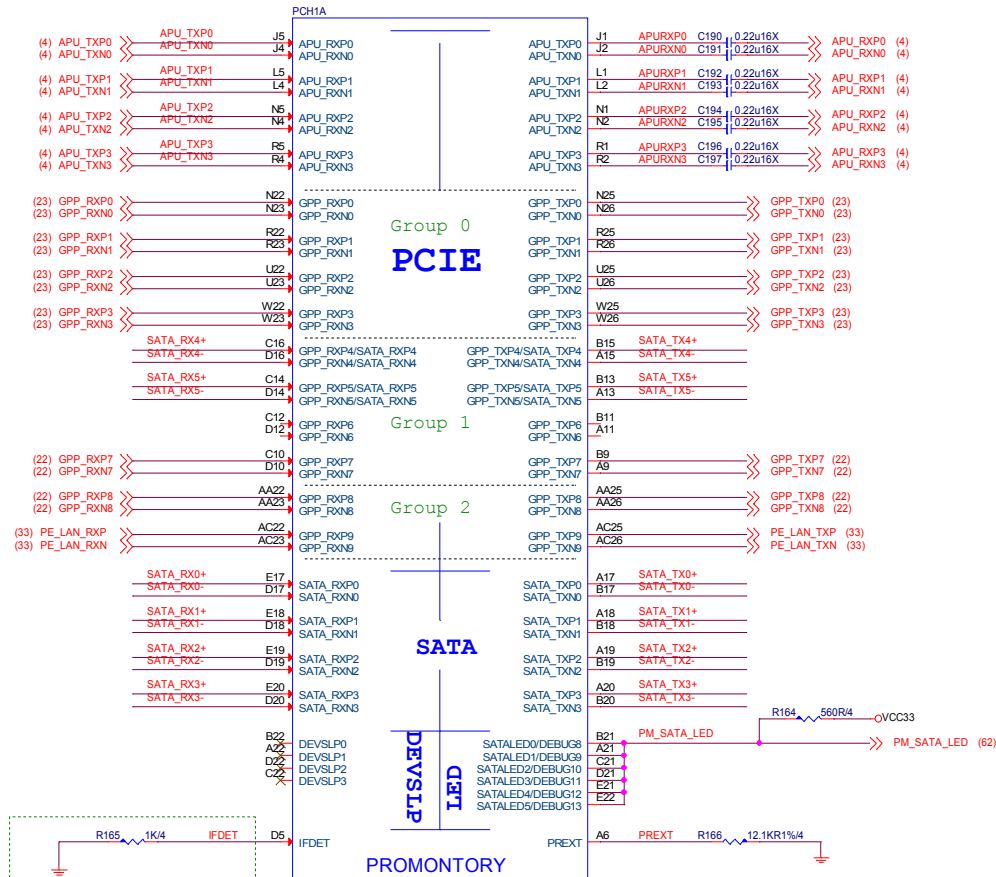
M2_2/PCI_E3 Share

SATA5_SATA6

PCI_E5

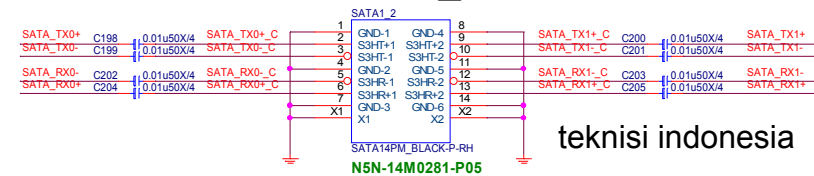
PCI_E2

LAN

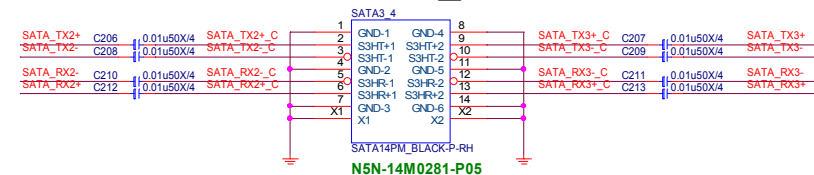


SATA Connector

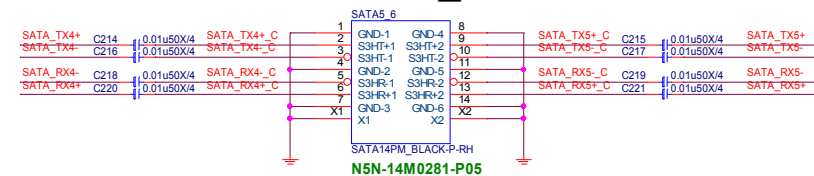
SATA1_2



SATA3_4



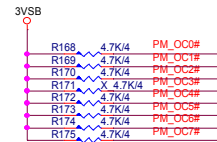
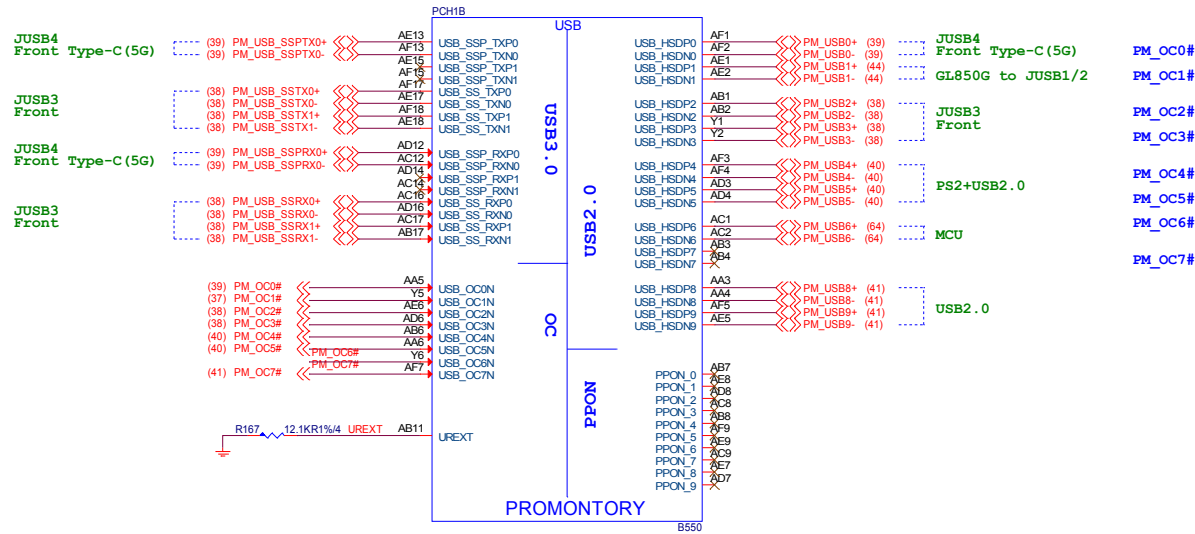
SATA5_6

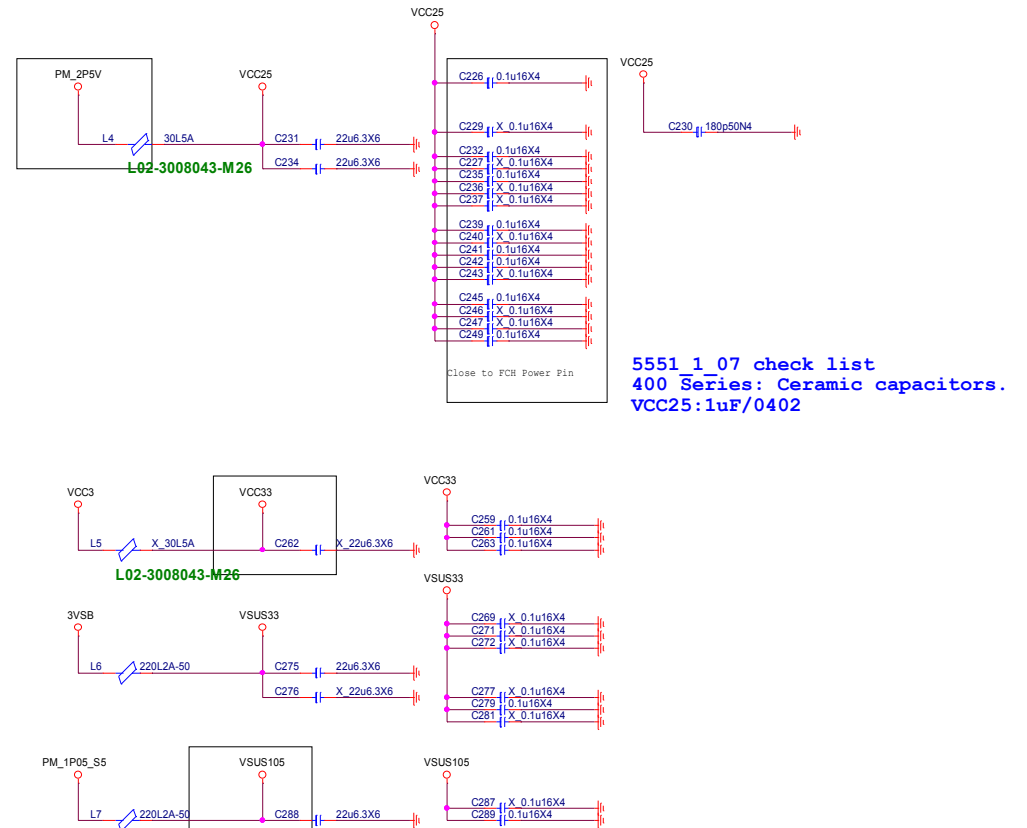
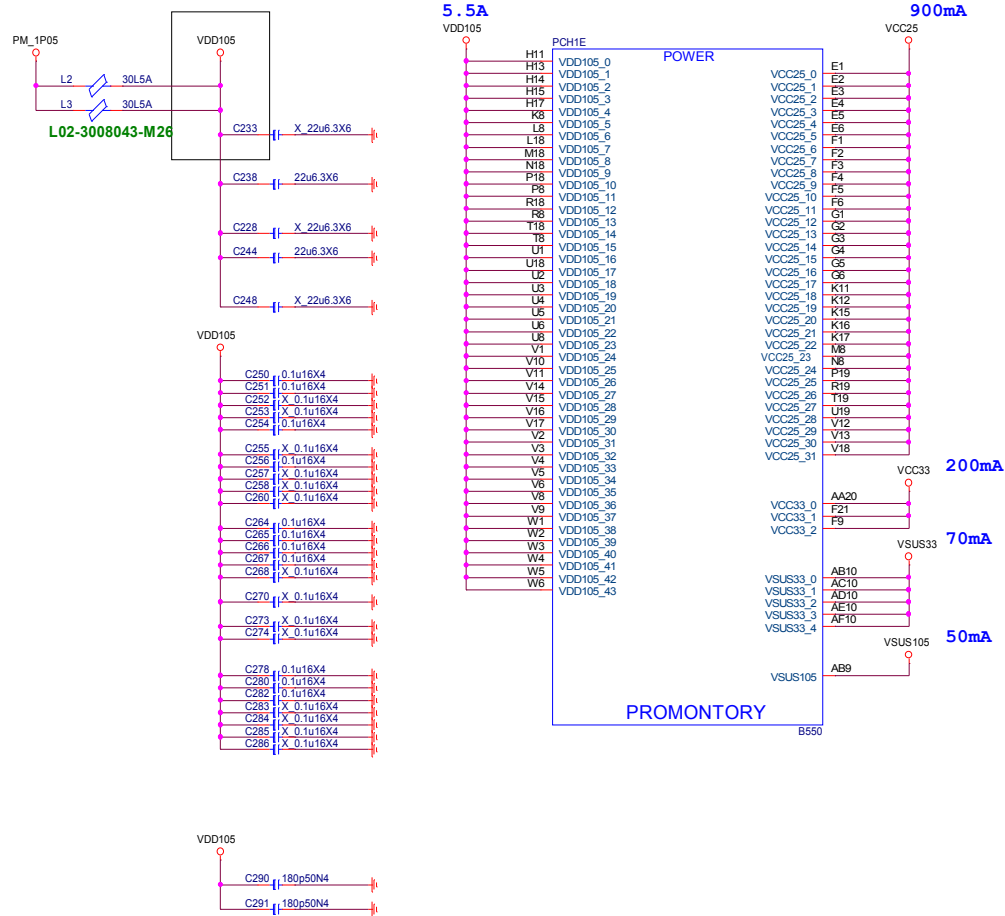


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Custom	Premium - PCIE/SATA	10
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GND

PROMONTORY



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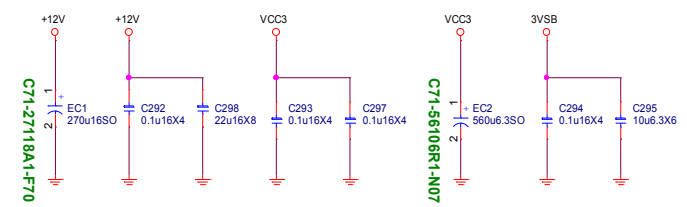
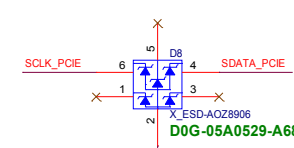
MS-7C56

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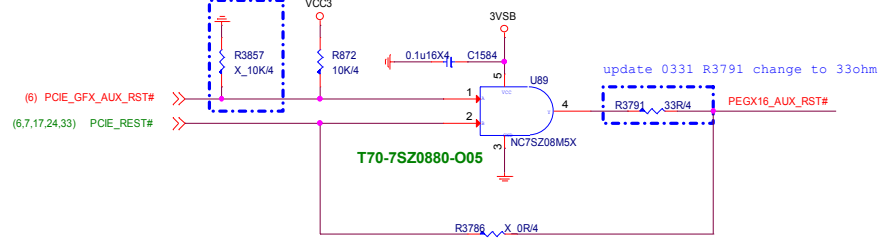
PCI EXPRESS x16 Slot

PCI_E1

SMB_SEL
GPIO Default High



update 0408 add pull down R38567



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Size Custom Document Description **PCI_E1 (X16)** Rev 10

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update 0331
net name change to PEDX16_WK#

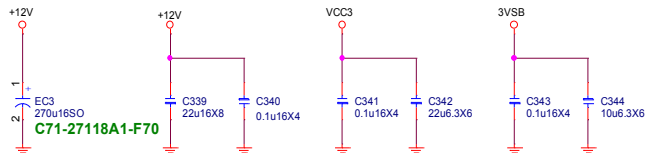
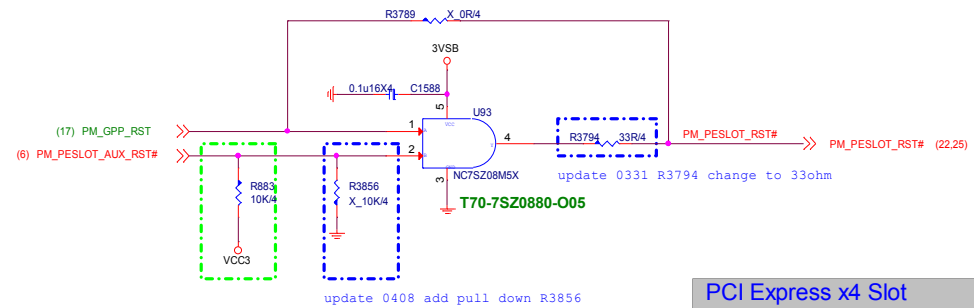
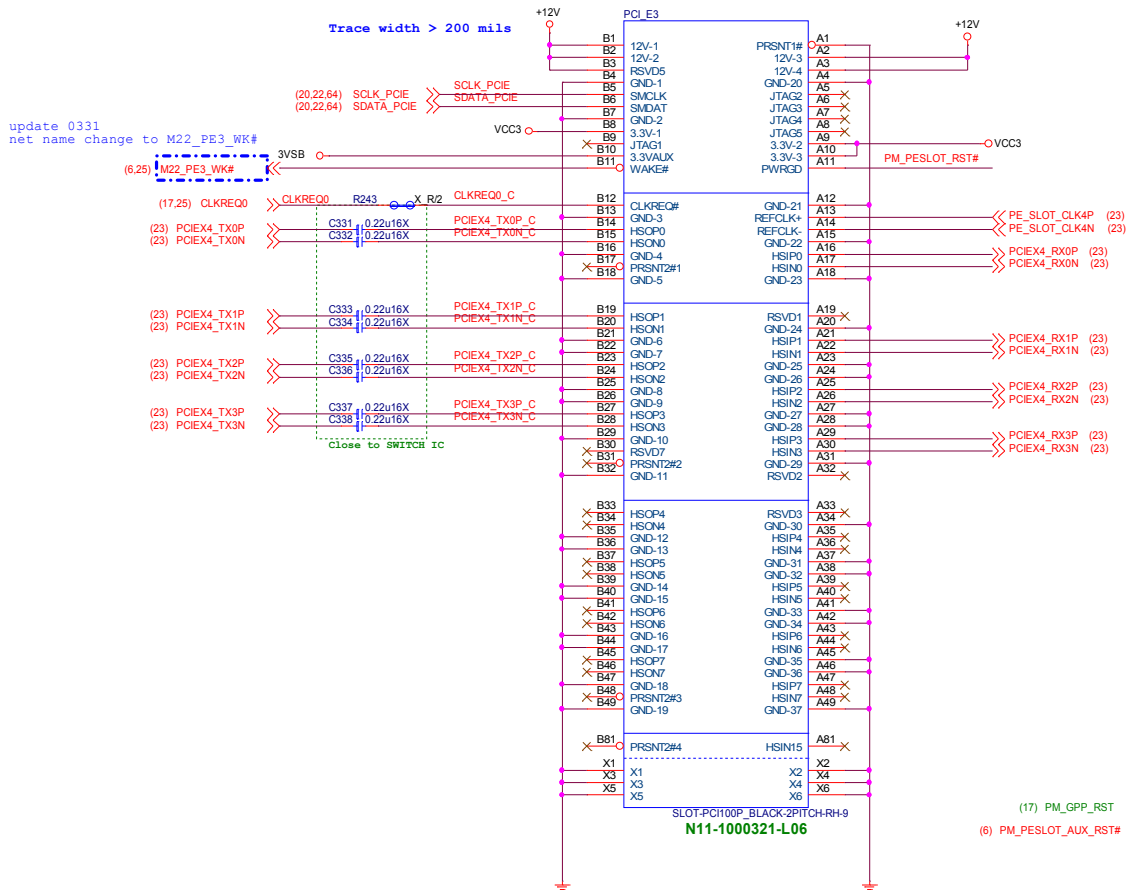


SLOT-PCI164P_BLACK-2PITCH-RH-73
N11-1641971-L06

PCI EXPRESS x4 SLOT

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PCI_E3 X4



PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD			
MS-7C56			
Size	Document Description	Rev	
Custom	PCI_E3 (X4)	10	
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PCI EXPRESS X1 SLOT

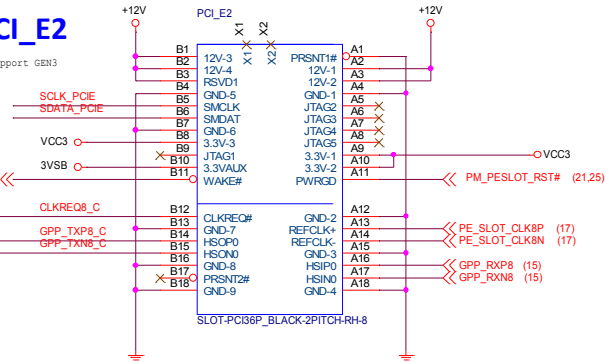
(20,21,64) SCLK_PCIE >> SCLK_PCIE
(20,21,64) SDATA_PCIE >> SDATA_PCIE

update 0331
net name change to PE4_PE5_WK#

(17) CLKREQ6 >> R245 X_R/2
(15) GPP_TXP8 >> C345 0.22u16X
(15) GPP_TXN8 >> C346 0.22u16X

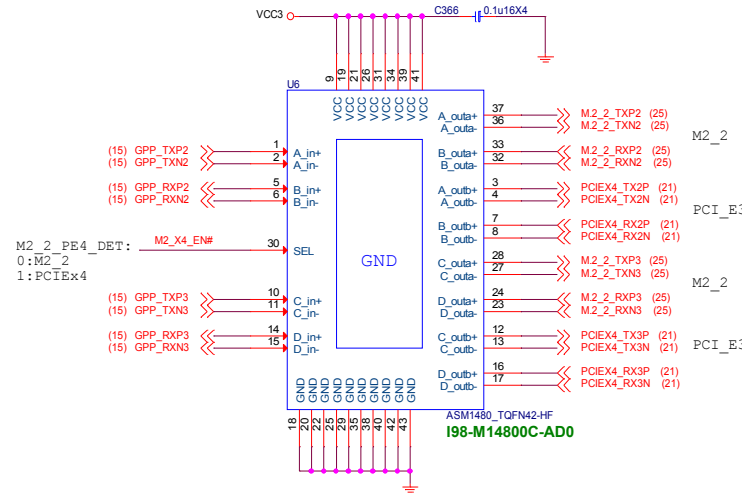
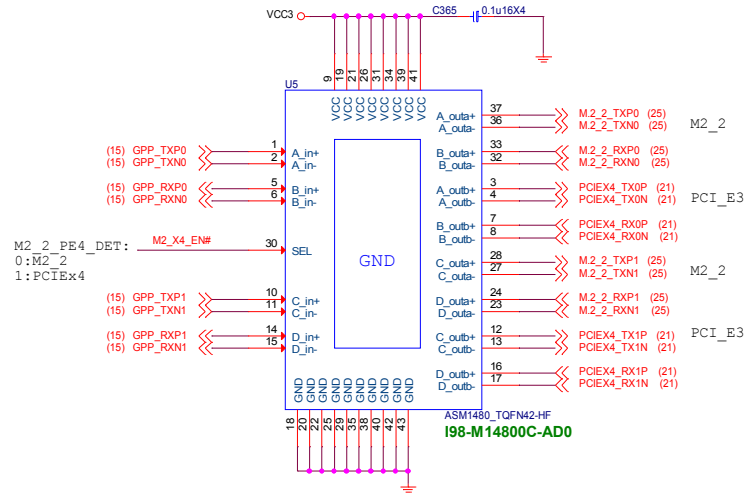
PCI_E2

support GEN3

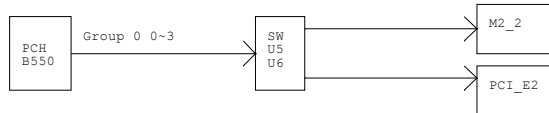
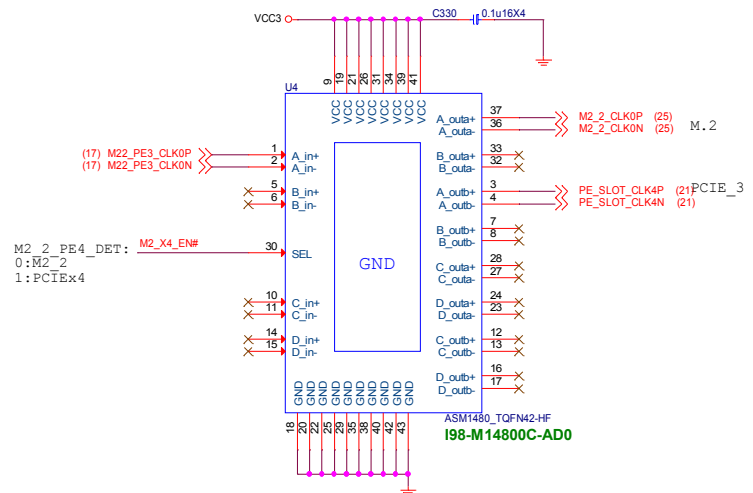
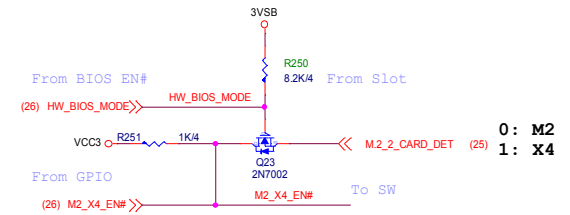


PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1.125A
+3V3_S5 (no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD			
MS-7C56			
Size Custom	Document Description	Rev 10	
Date: Monday, May 04, 2020		Sheet 22	of 75



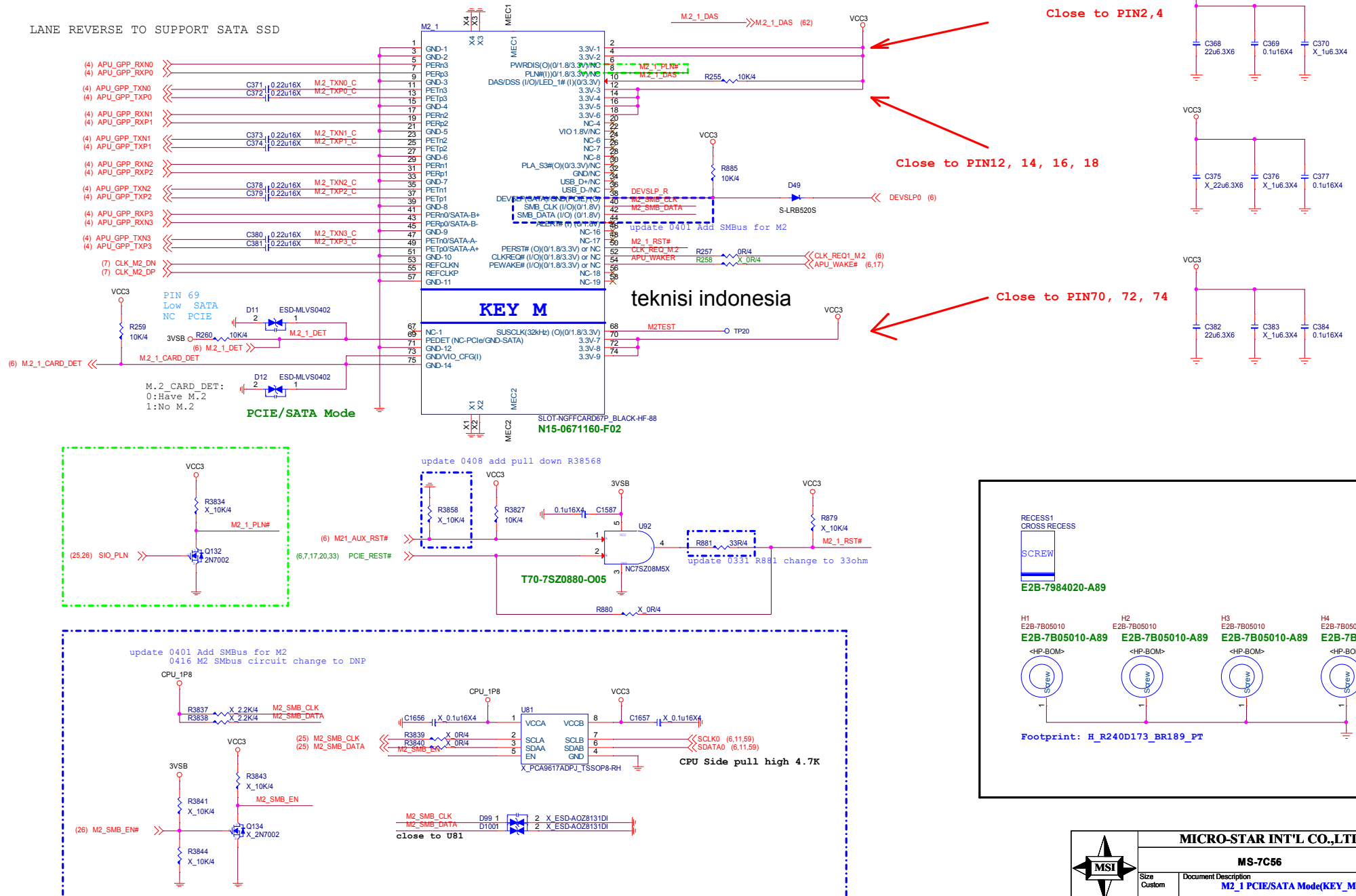
PCIe Lanes control circuit



	MICRO-STAR INT'L CO.,LTD		
	MS-7C56		
	Size Custom	Document Description PCIe GEN3 SWITCH	Rev 10
	Date: Monday, May 04, 2020	Sheet 23 of 75	

VCC3 4.25A
Max: 14W

LANE REVERSE TO SUPPORT SATA SSD



MICRO-STAR INT'L CO.,LTD

MS-7C56

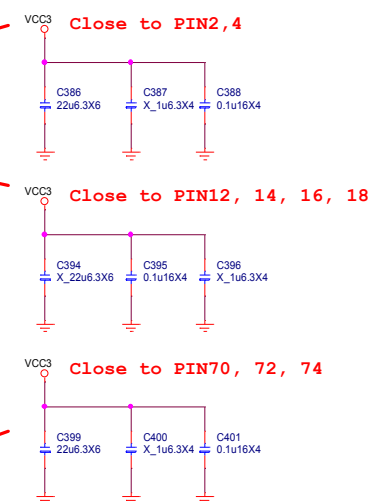
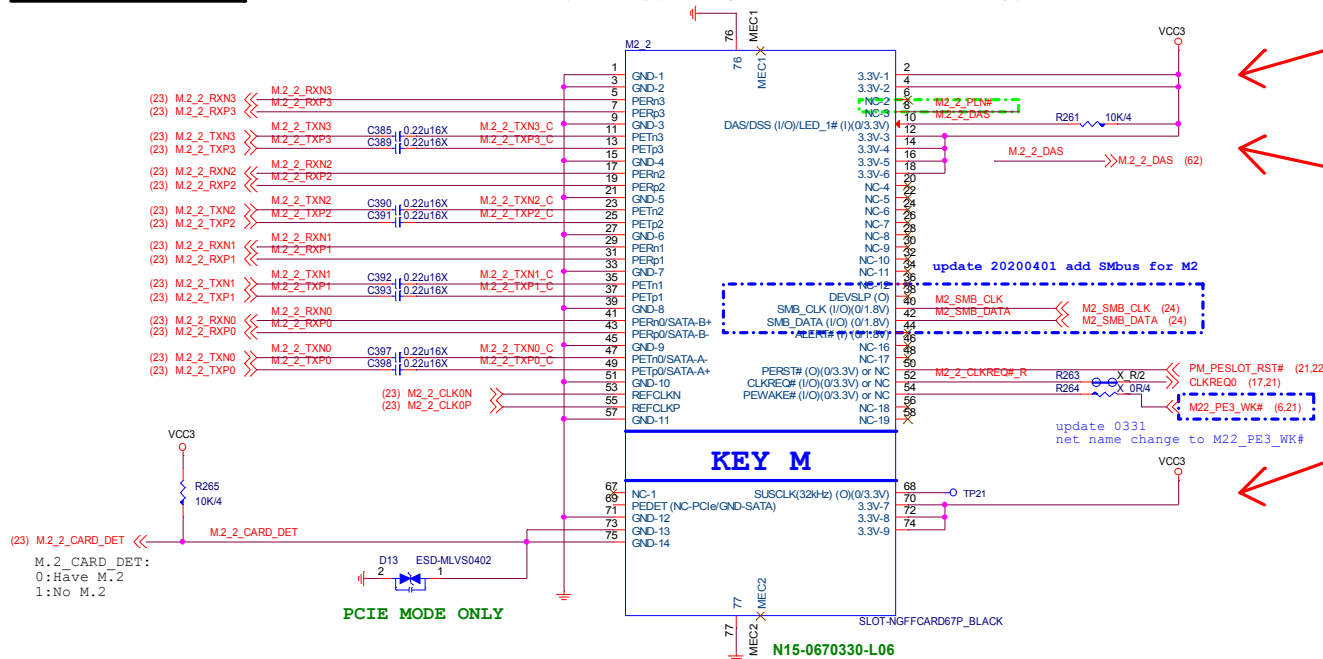
Size	Document Description
Custom	M2_1 PCIE/SATA Mode(KEY_M)

Date: Monday, May 04, 2020 Sheet 24 of 75

M.2_2 Connector

M2下方零件擺放限高要小於0.9mm的零件

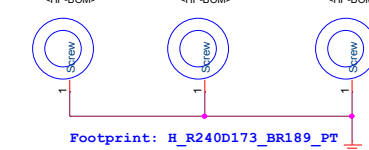
VCC3 4.25A
Max: 14W



RECESS2
CROSS RECESS
E2B-7984020-A89



H5 H6 H7
E2B-7B05010 E2B-7B05010 E2B-7B05010
E2B-7B05010-A89 **E2B-7B05010-A89** **E2B-7B05010-A89**
SHP-ROHS SHP-ROHS SHP-ROHS



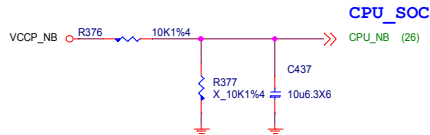
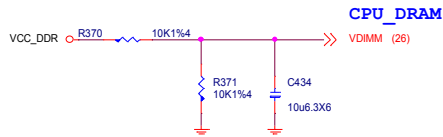
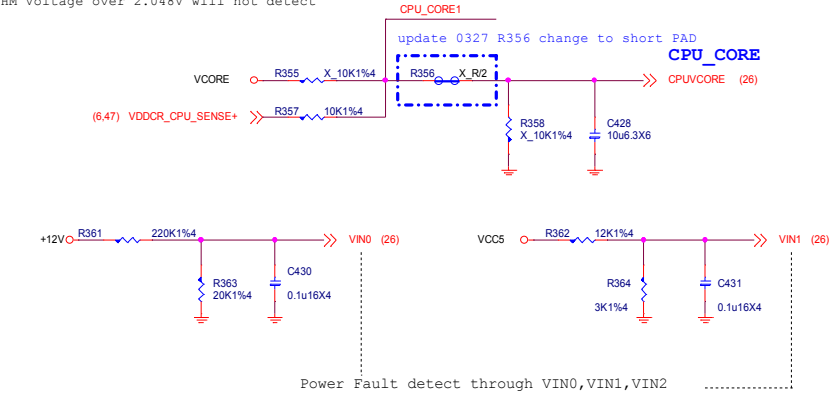
MICRO-STAR INT'L CO.,LTD

MS-7C56

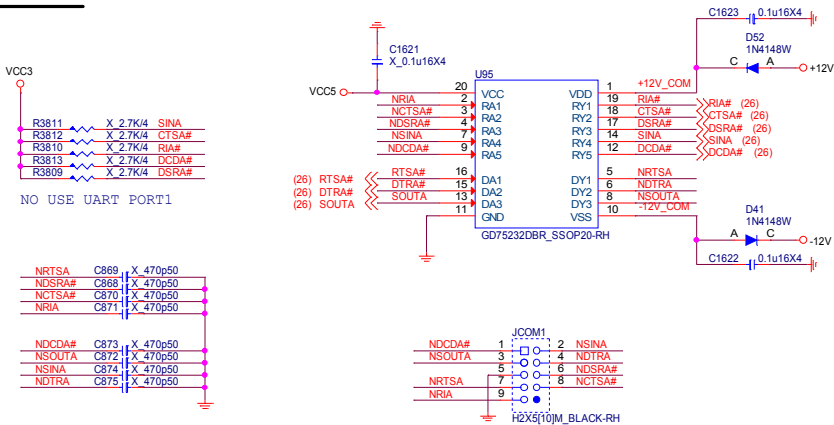
Size Custom	Document Description M2_2 PCIE Mode(KEY_M)	Rev 10
Date: Monday, May 04, 2020		Sheet 25 of 75

HW Monitor - Voltage

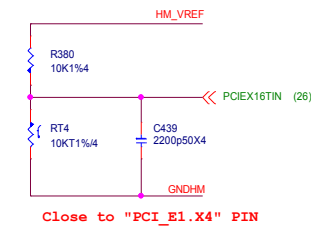
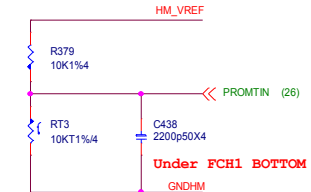
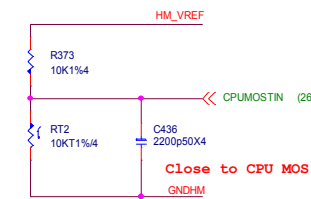
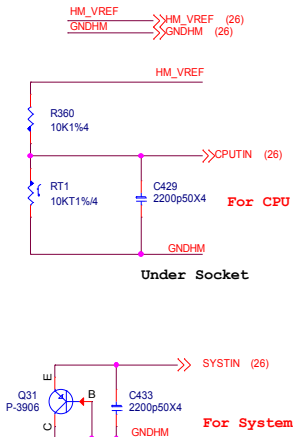
SIO HM Voltage over 2.048V will not detect



COM 1



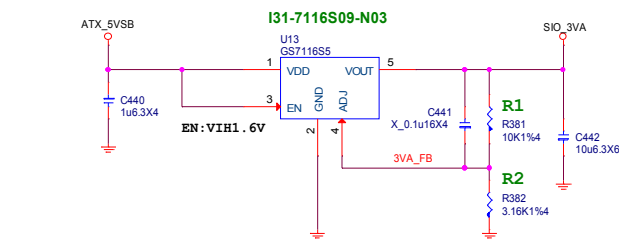
TEMP SENSOR



PM RESET

CPU RESET

SIO_3VA

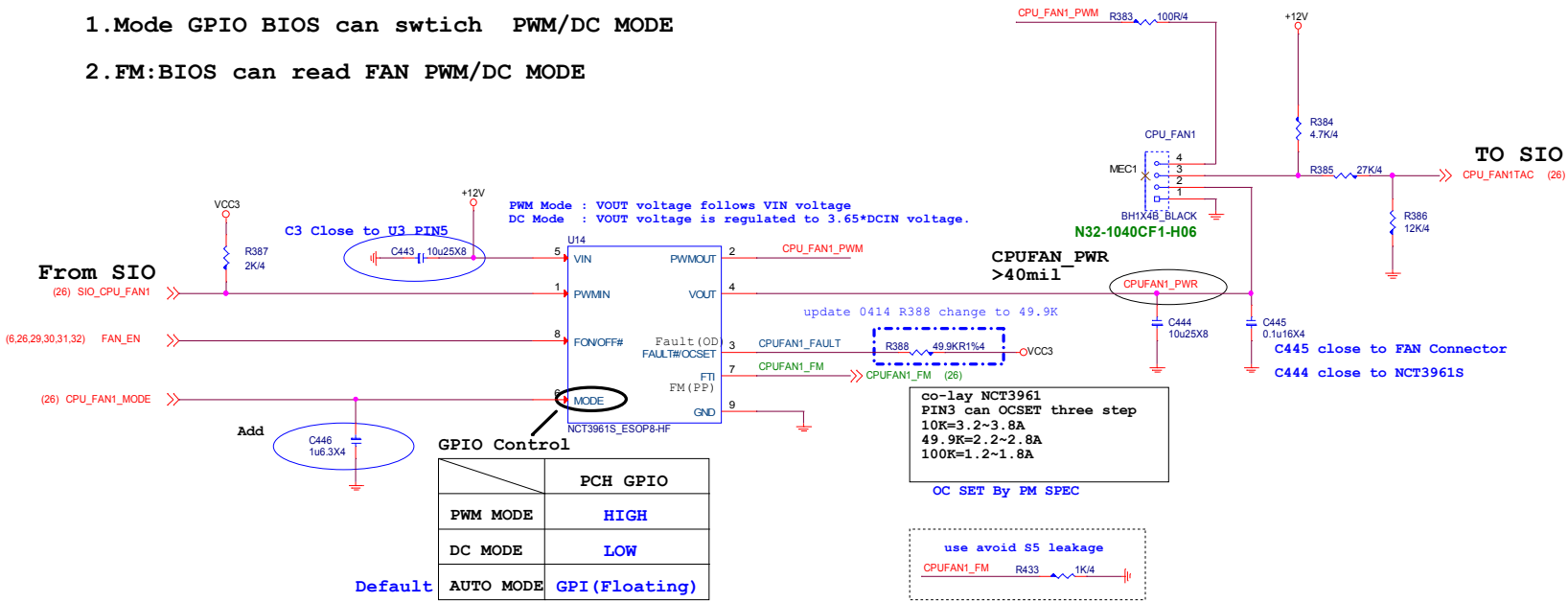


$$V_{out} = V_{ref} * (1 + (R1/R2)) = 0.8 * (1 + (10K/3.16K)) = 3.33V$$

MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description SIO - HW Monitor/COM	Rev 10
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CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

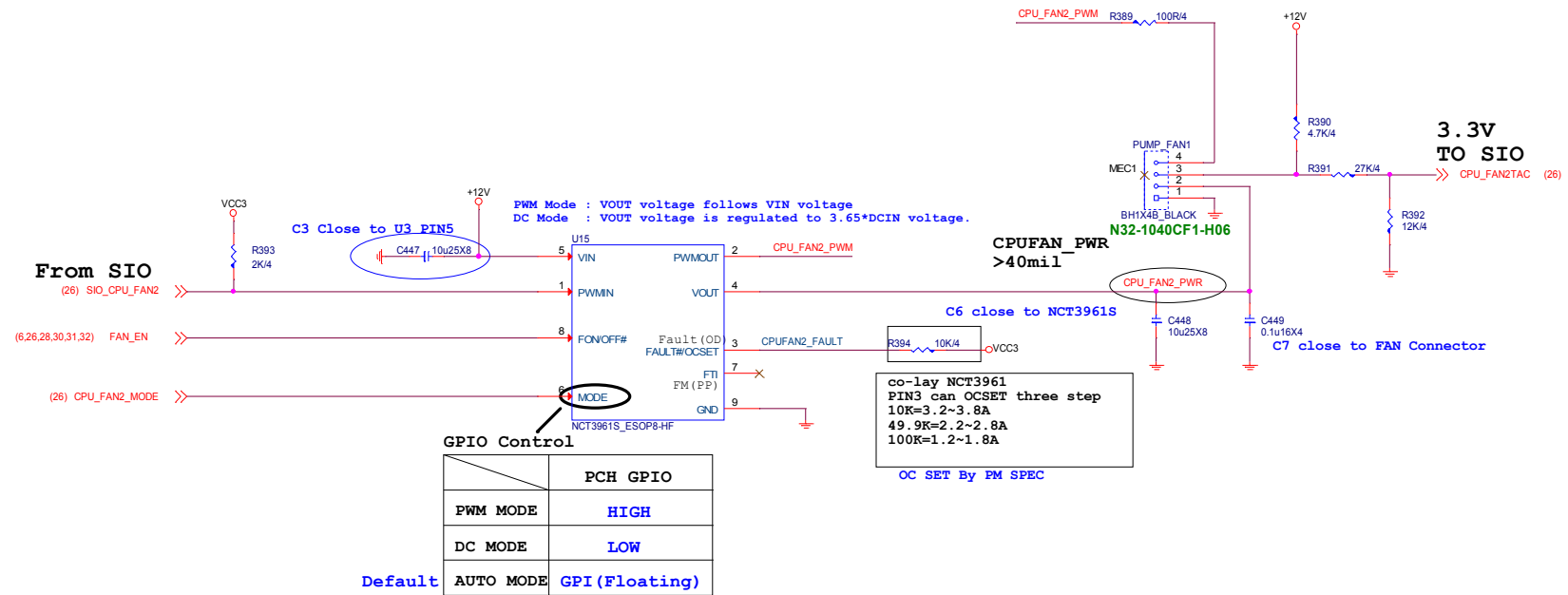
- 1.Mode GPIO BIOS can switch PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



PUMPFAN1

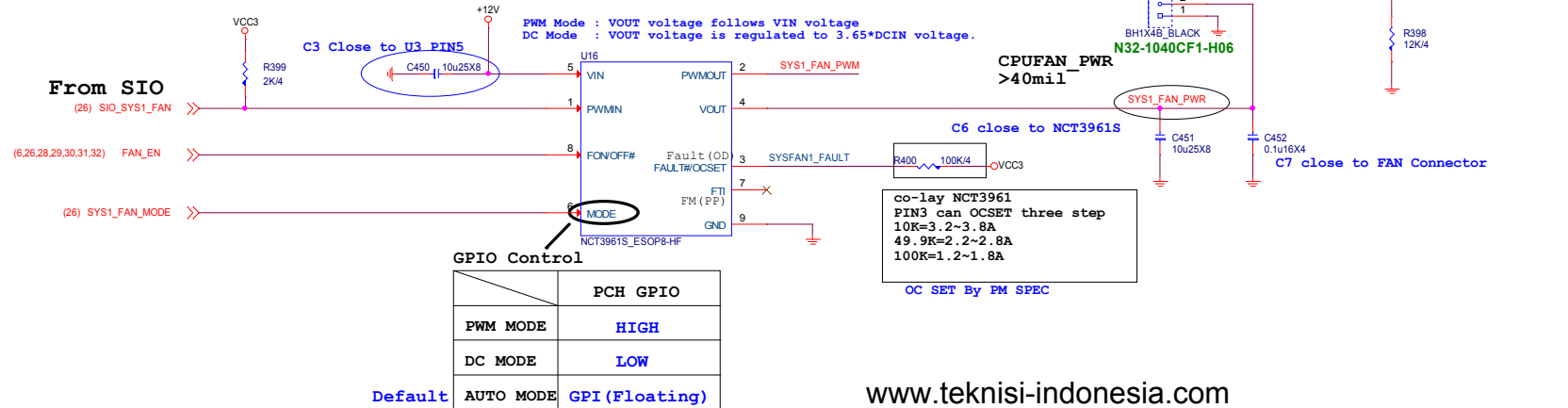
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



```
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE
```

1.Mode GPIO BIOS can swtich PWM/DC MODE

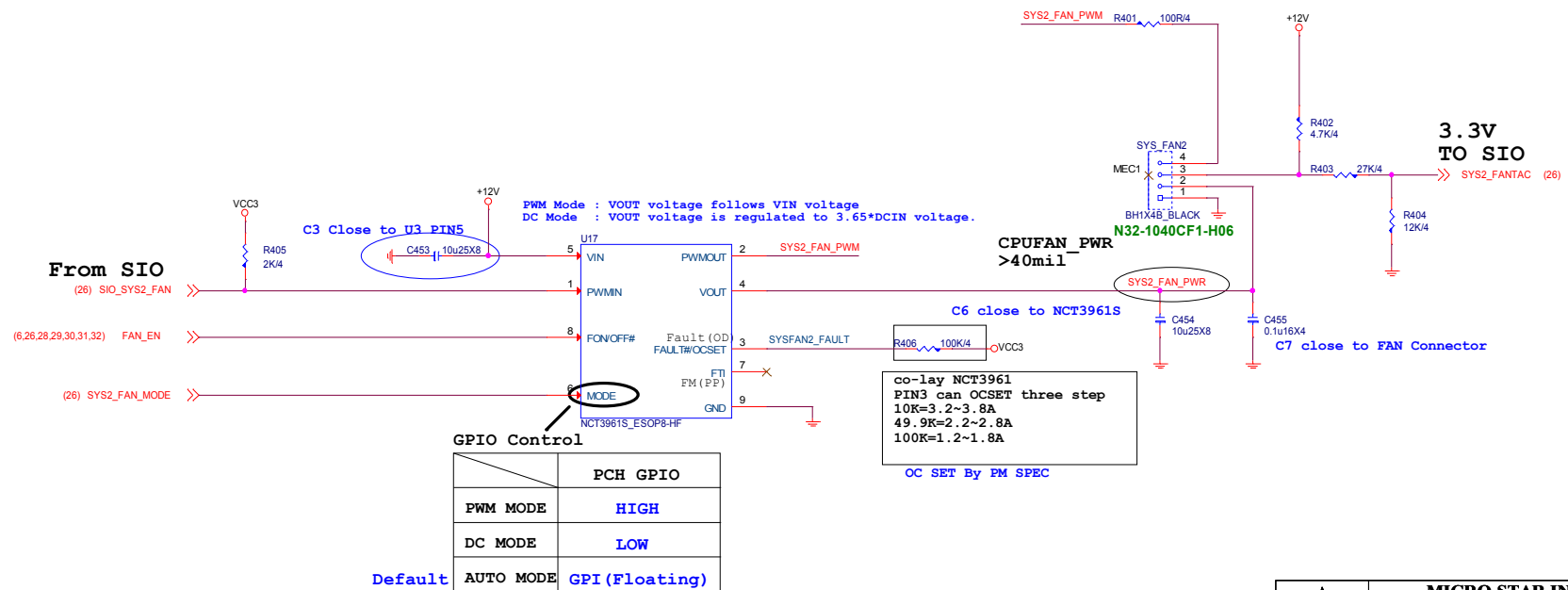


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SYSFAN2

```
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE
```

1.Mode GPIO BIOS can swtich PWM/DC MODE



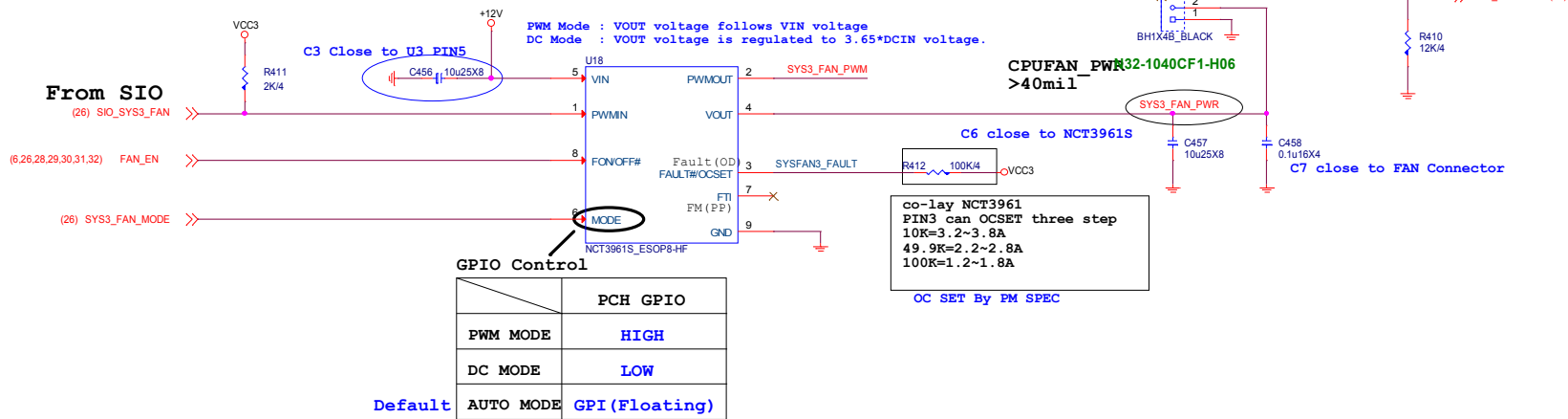
MICRO-STAR INT'L CO.,LTD

MS-7C56

Size Custom	Document Description FAN TYPE-K SYSFAN1/2	Rev 10
Date: Monday, May 04, 2020	Sheet 30 of 75	

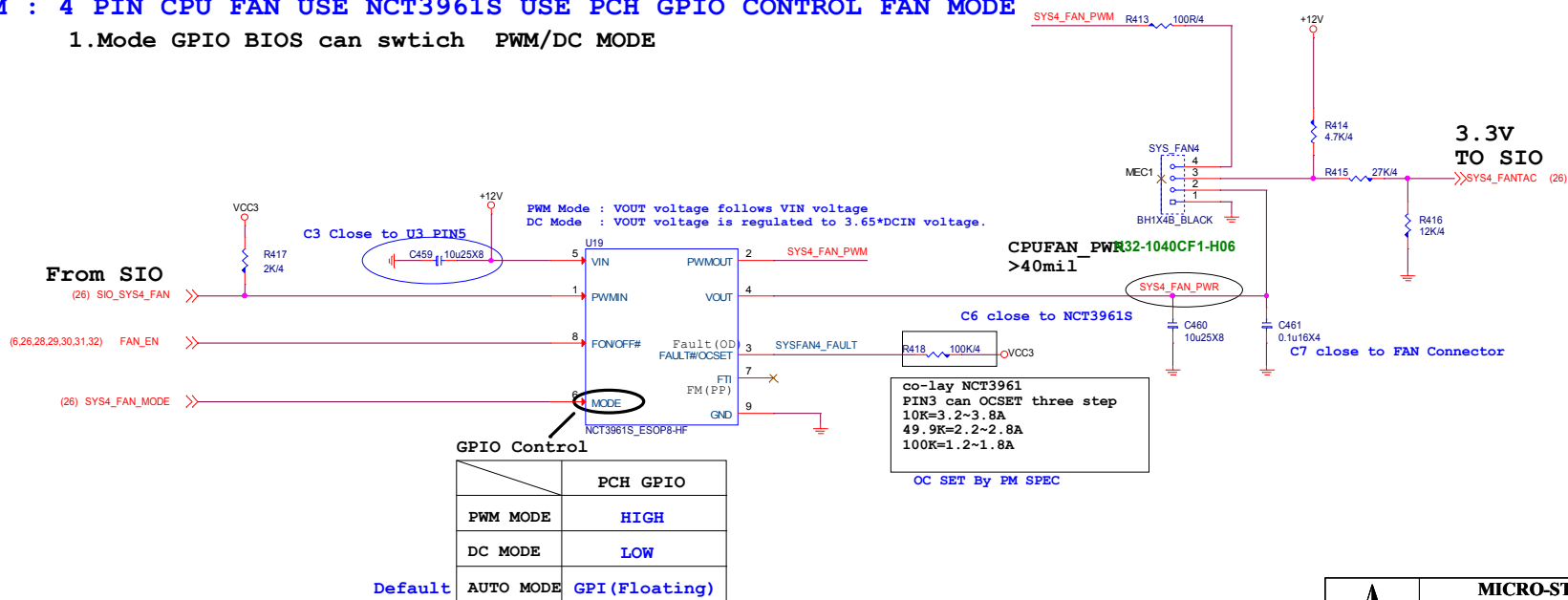
SYSFAN3 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



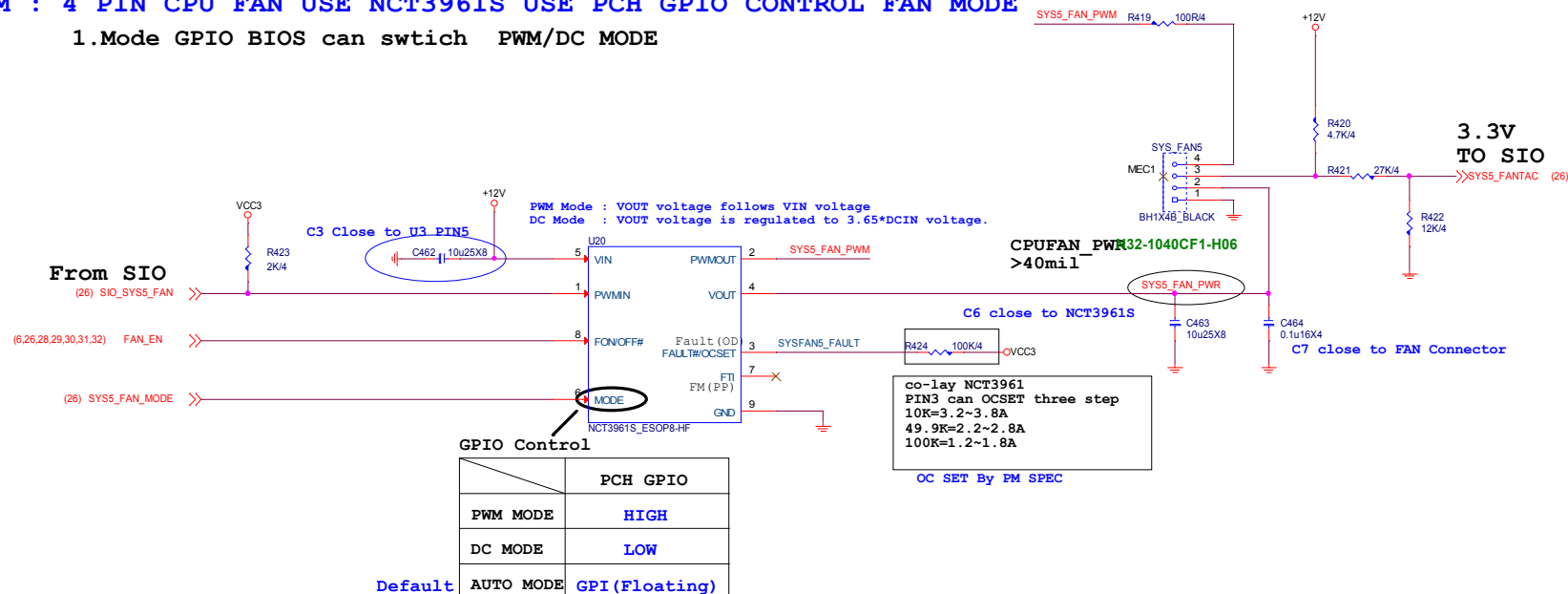
SYSFAN4 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



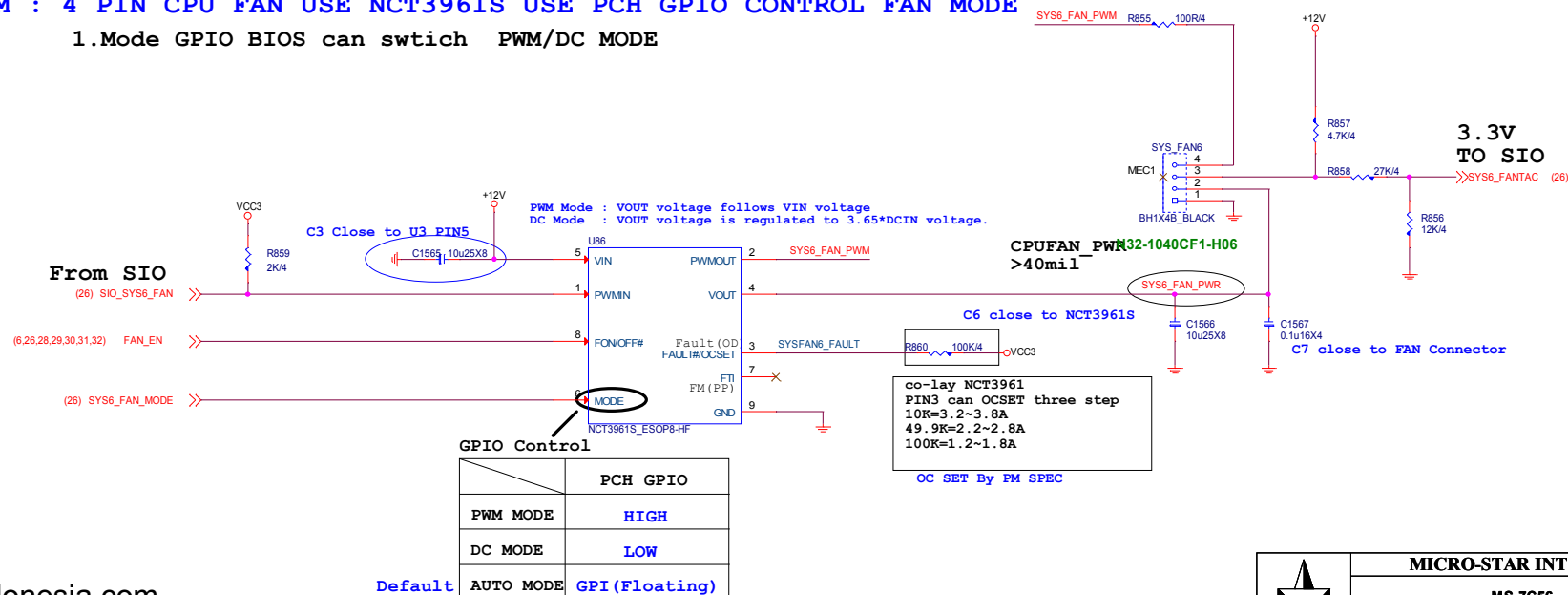
SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



RTL8111H Giga LAN

8111H: B06-08111CC-R09
8111G: B06-081116C-R09

update 0331
 net name change to LAN_WK#
 (6) LAN_WK#
 (26) SIO_LAN_WAKE#

update 0408 add pull down R3859

update 0331 add R3846

2015.06.22

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

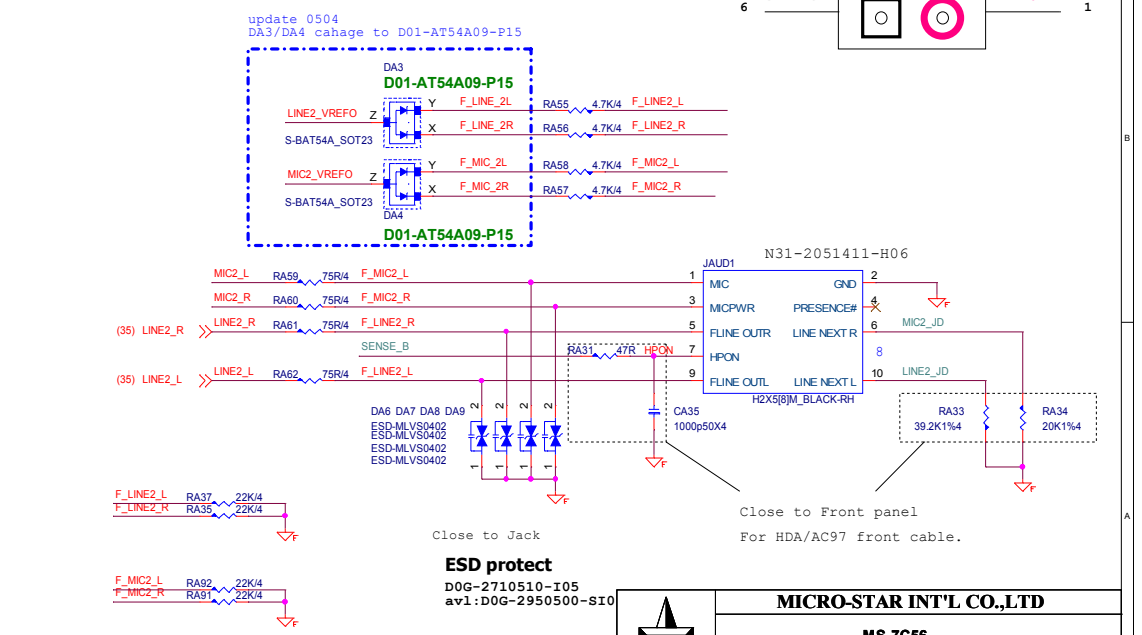
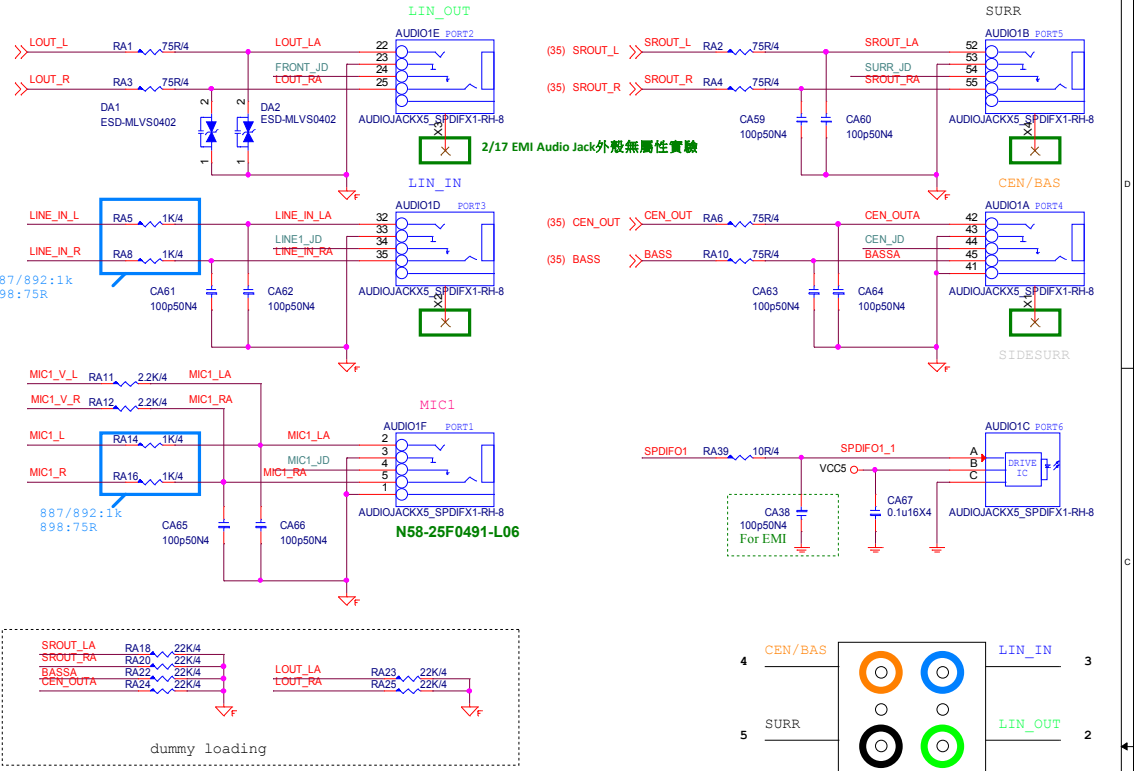
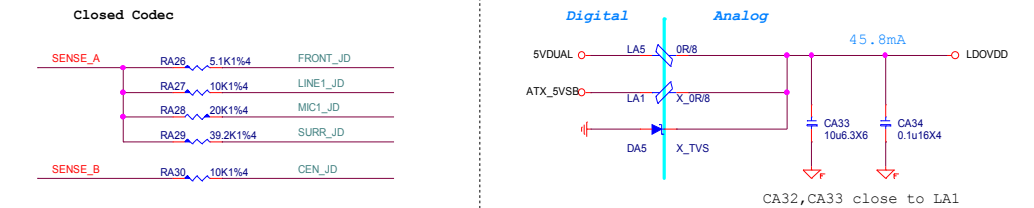
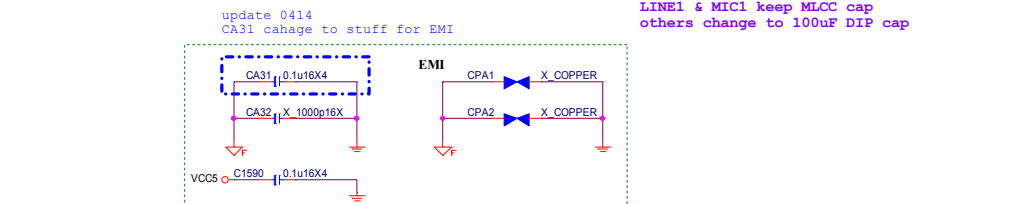
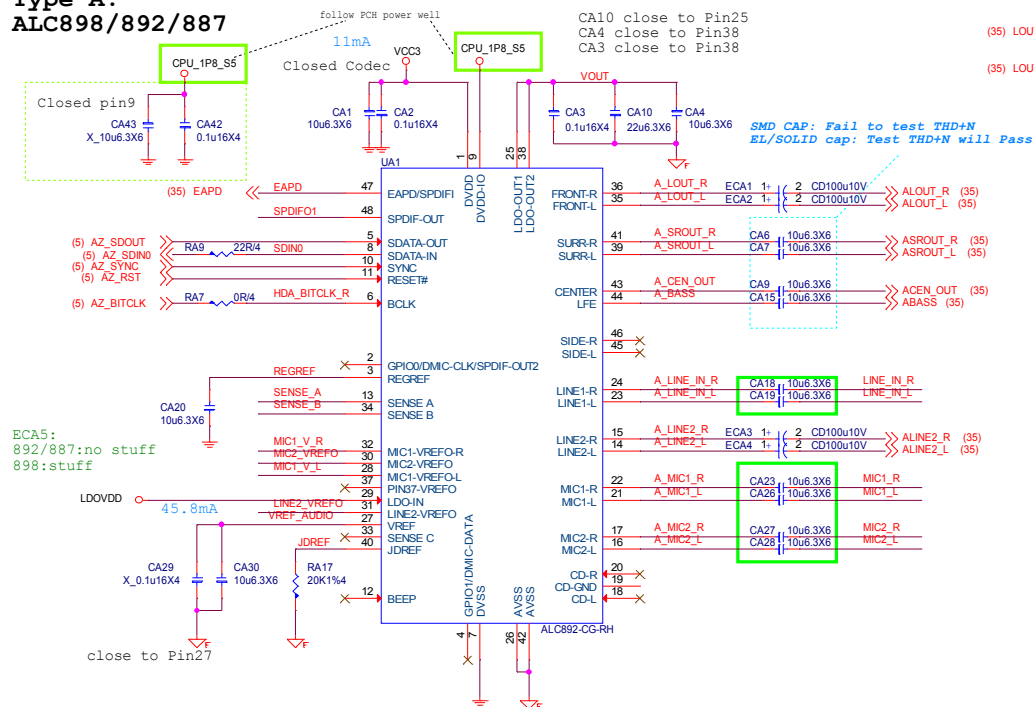
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

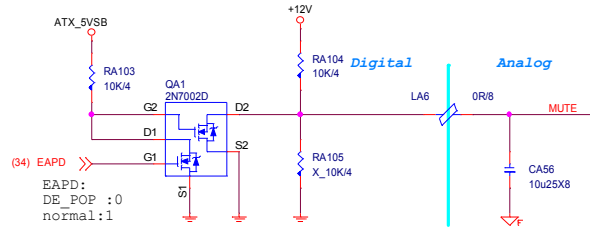
ESD Protect
 UL2&UL3 close to connector

MSI
MICRO-STAR INT'L CO.,LTD
MS-7C56
 Size Custom Document Description LAN - RTL8111H Rev 10
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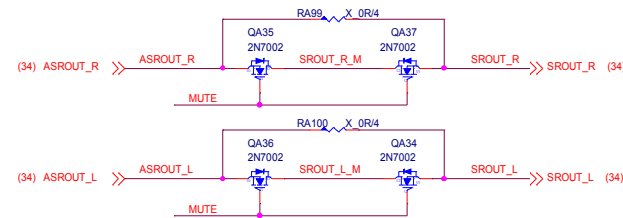
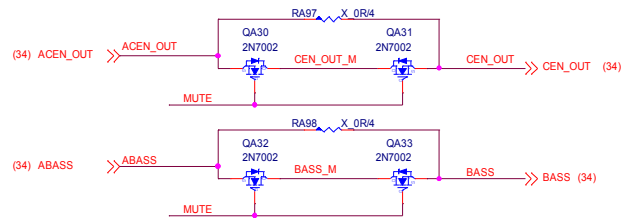
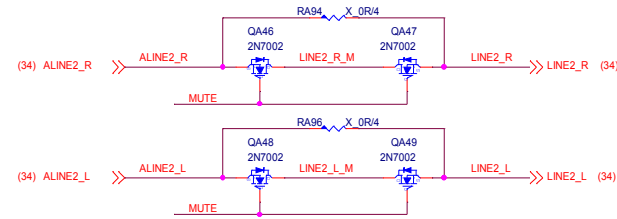
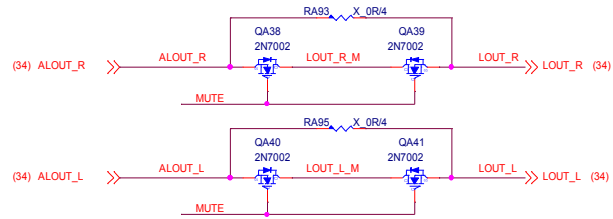
Type A:
ALC898/892/887



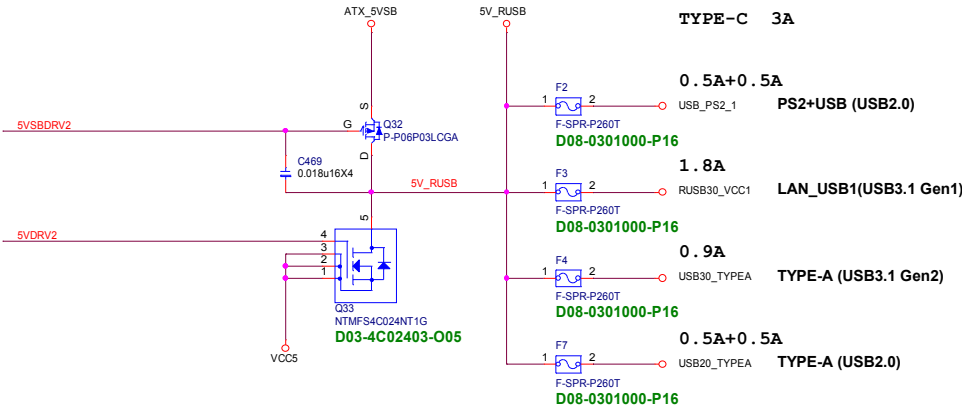
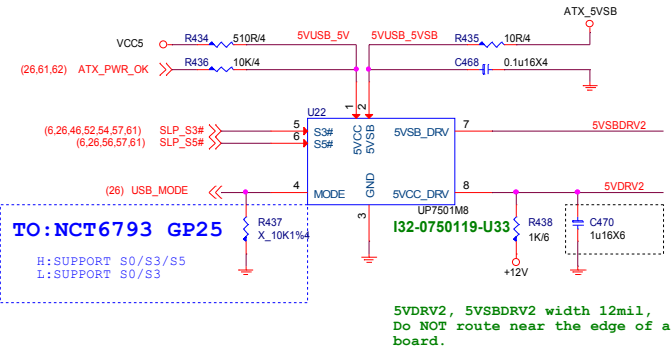
De-POP circuit



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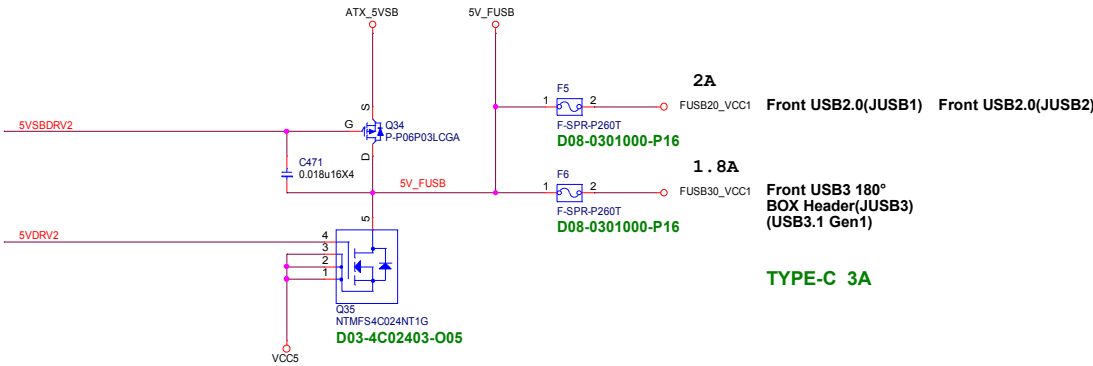


USB Power



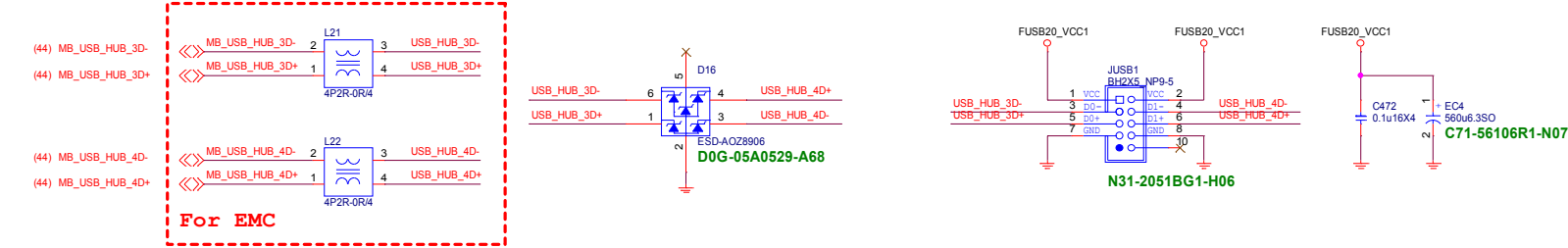
Rear (7.7A)

Front (6.8A)



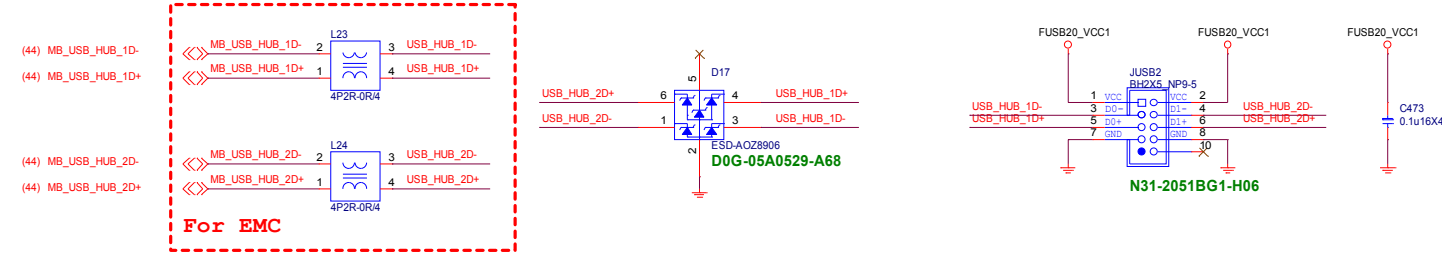
Front USB2.0 (JUSB1) Form GL850G USB2.0 HUB

5V@1A

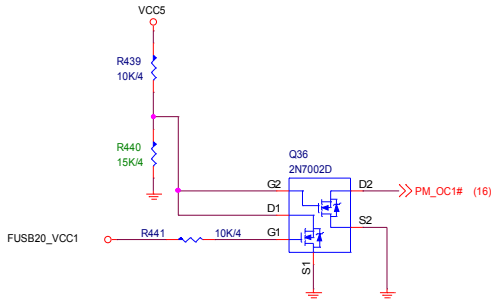


Front USB2.0 (JUSB2) Form GL850G USB2.0 HUB

5V@1A



Front USB2.0 OC



**Front USB3 180°
BOX Header(JUSB3)
5V@1.8A**

(16) PM_USB2+ <<> PM_USB2+
(16) PM_USB2- <<> PM_USB2-

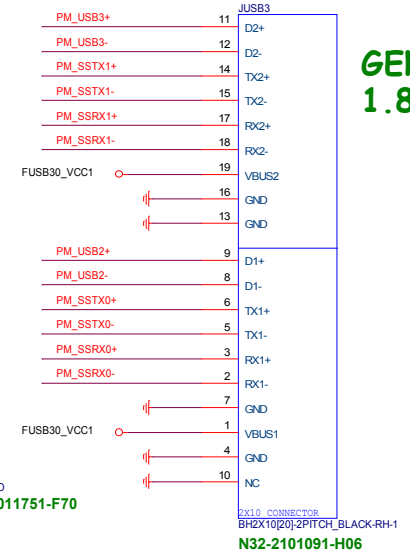
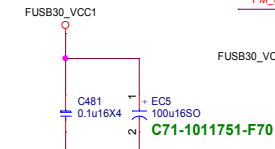
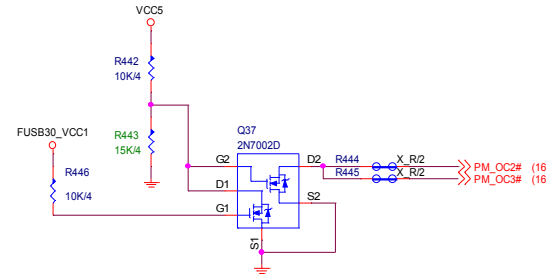
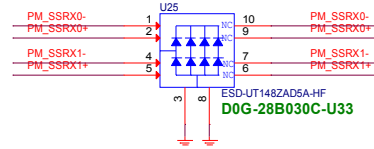
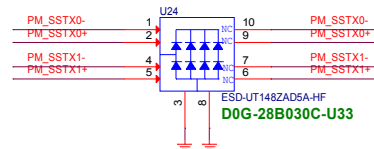
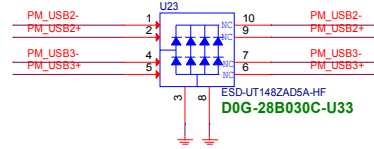
(16) PM_USB3+ <<> PM_USB3+
(16) PM_USB3- <<> PM_USB3-

(16) PM_USB_SSTX0+ <<> C474 0.22u16X PM_SSTX0+
(16) PM_USB_SSTX0- <<> C475 0.22u16X PM_SSTX0-

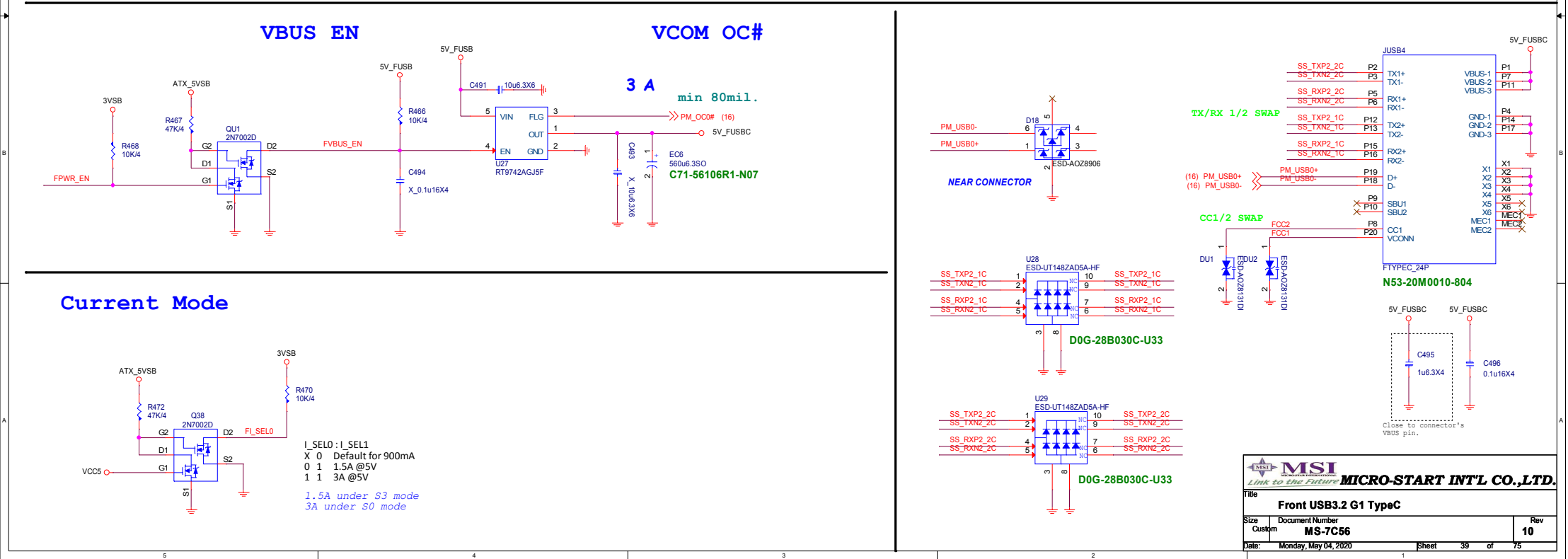
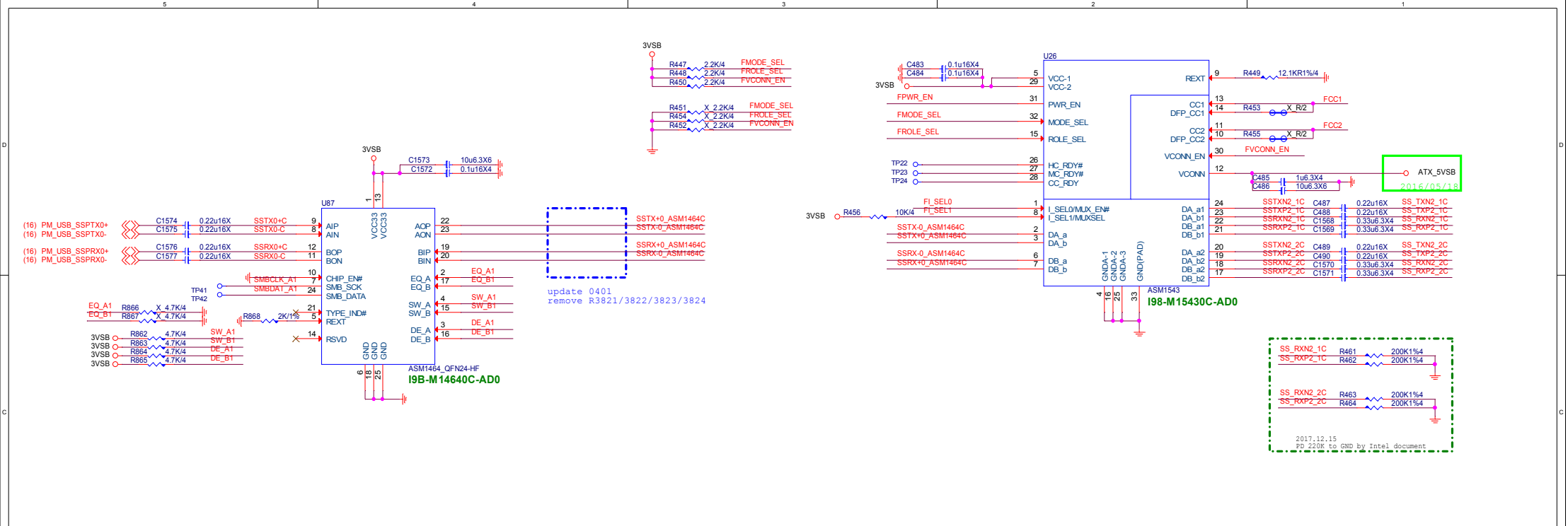
(16) PM_USB_SSRX0+ <<> C476 0.33u6.3X4 PM_SSRX0+
(16) PM_USB_SSRX0- <<> C477 0.33u6.3X4 PM_SSRX0-

(16) PM_USB_SSTX1+ <<> C478 0.22u16X PM_SSTX1+
(16) PM_USB_SSTX1- <<> C479 0.22u16X PM_SSTX1-

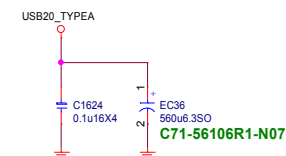
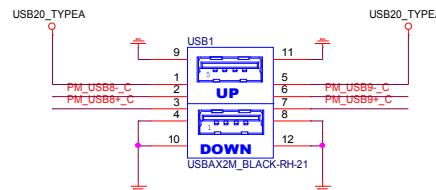
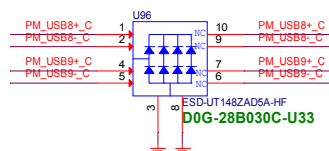
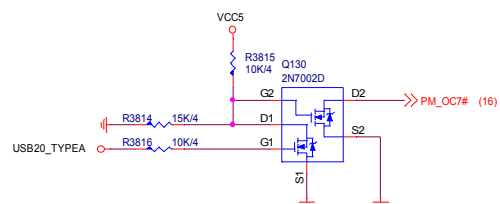
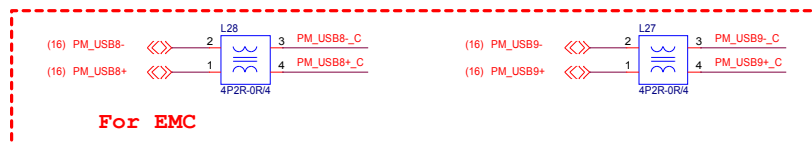
(16) PM_USB_SSRX1+ <<> C480 0.33u6.3X4 PM_SSRX1+
(16) PM_USB_SSRX1- <<> C482 0.33u6.3X4 PM_SSRX1-



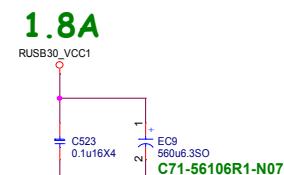
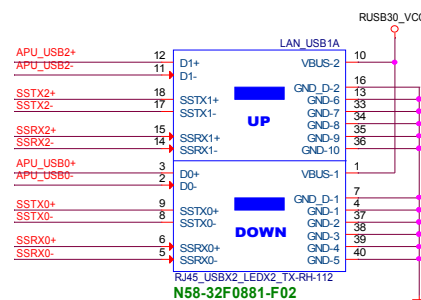
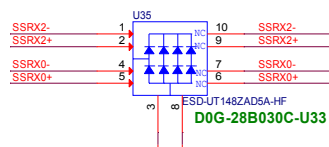
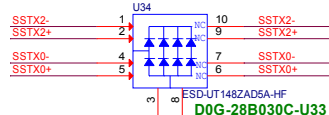
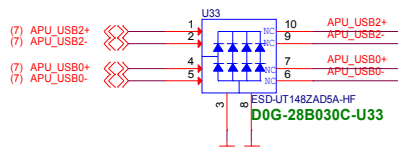
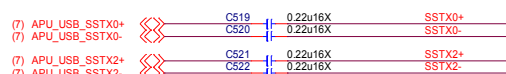
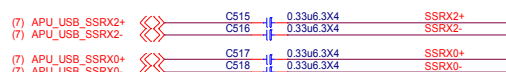
**GEN1
1.8A**



Rear USB2.0 5V@0.5A+0.5A

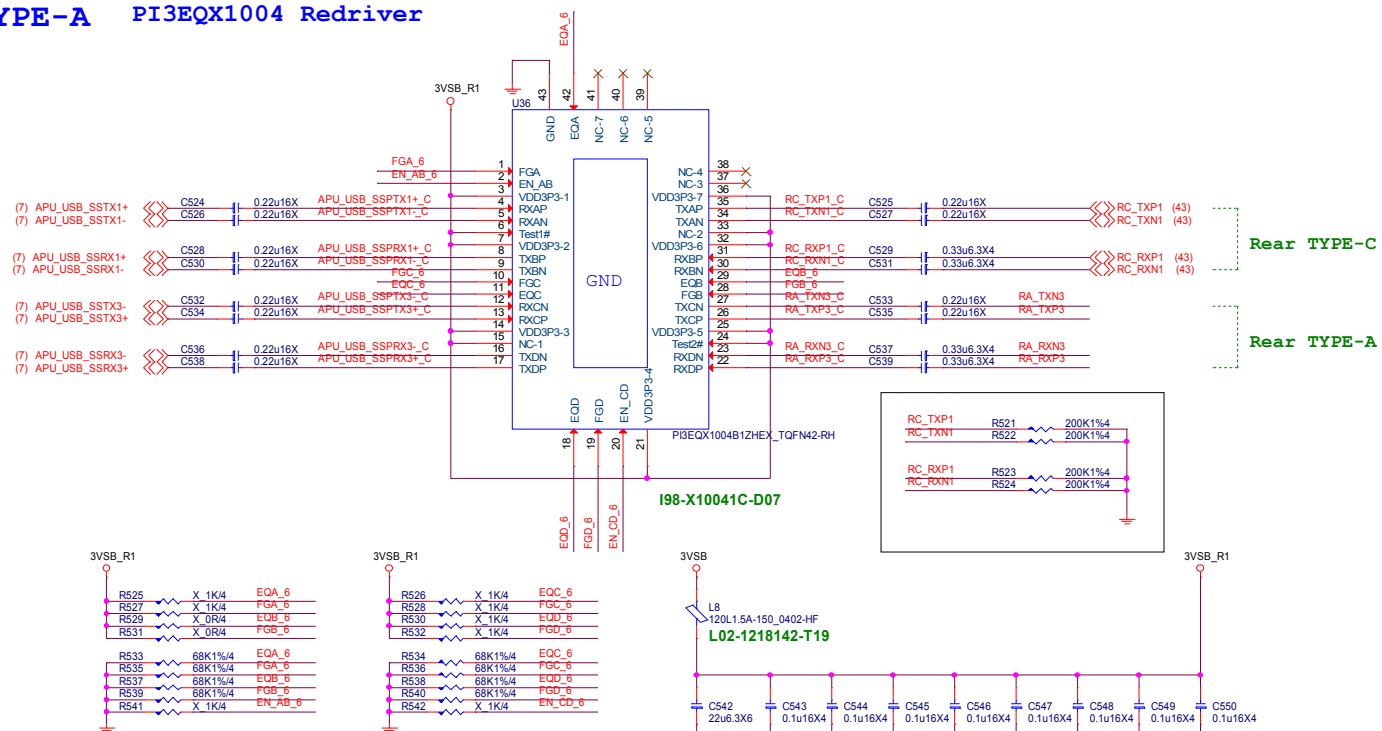


Rear USB3.1 GEN1 5V@1.8A



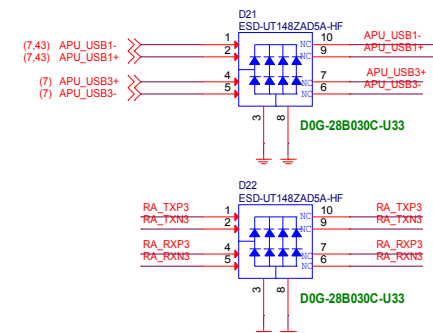
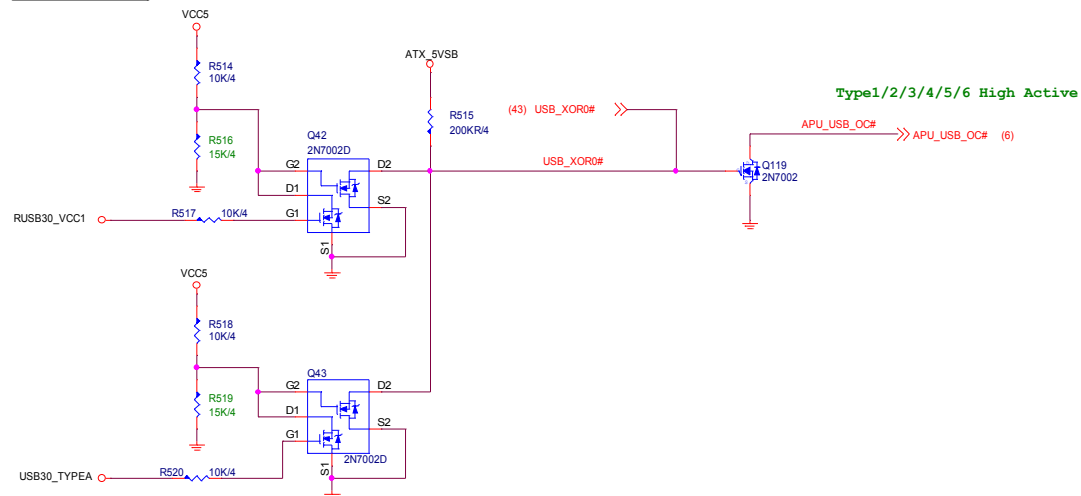
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Custom	Rear USB3.2 G1 / USB2.0	10	
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TYPE-A PI3EQX1004 Redriver

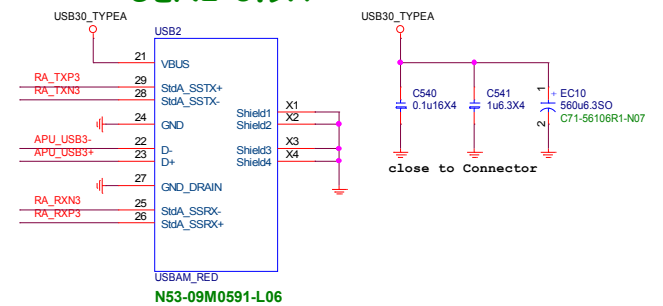


EQ	dB				EQ	FG	FG	dB	
0	10.9	0 to GND	APU_USB_SSTX1	A	R	R	0	-3	0 to GND
R	6.7	68K to GND	APU_USB_SSRX1	B	R	R	R	-1.5	68K to GND
F	8.9	NC	APU_USB_SSTX3	C	R	R	F	0	NC
1	13.1	0 to VDD	APU_USB_SSRX3	D	R	R	1	2	0 to VDD

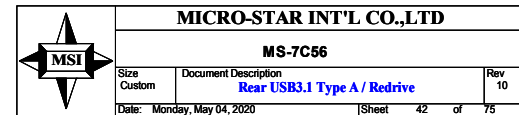
CPU USB_OC



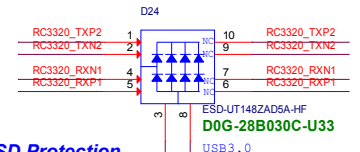
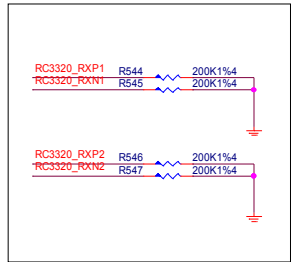
GEN2 0.9A



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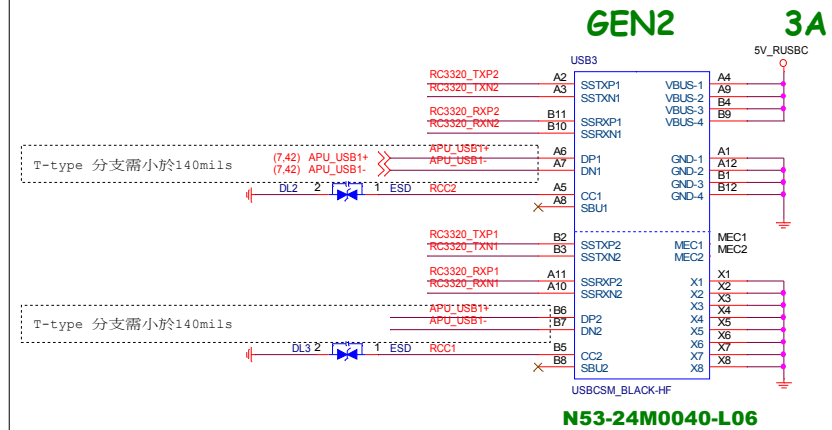


USB Type-C MUX with Configuration Channel (CC)

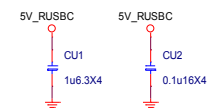
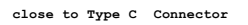


USB3.0
DOG-06A050C-A68 Main
DOG-05A0300-I14 AVL
DOG-45B031C-O05 AVL

VBUS EN



Current Mode

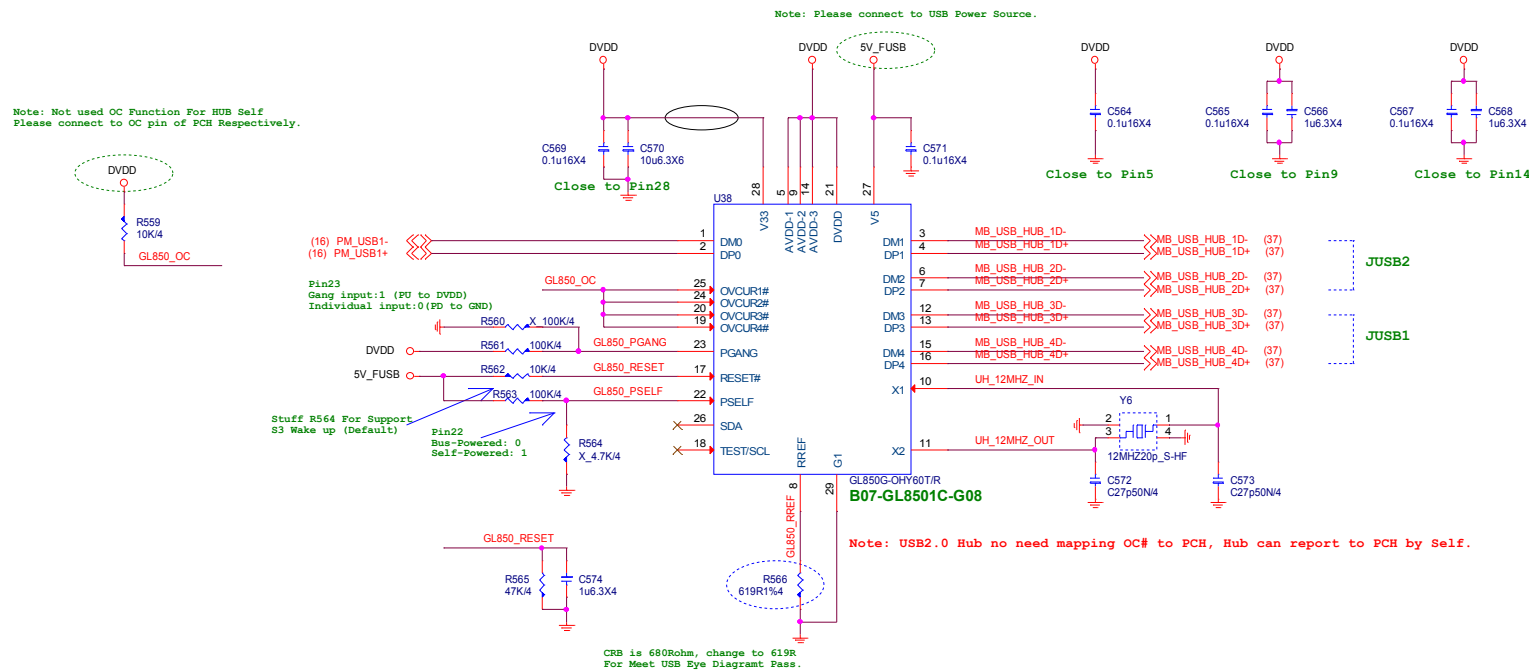


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Size Custom	Document Description Rear USB3.1 Type C / mux	Rev 10
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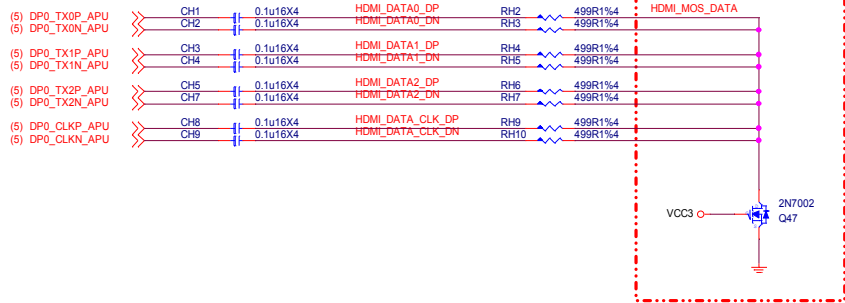
GL850G USB2.0 HUB

5V_FUSB

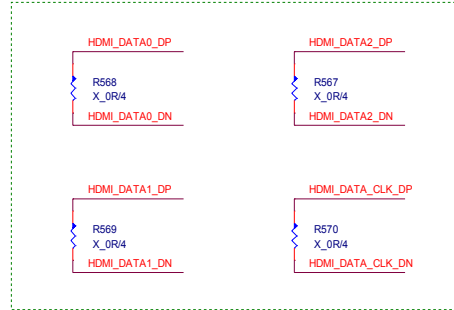


HDMI CONNECTOR

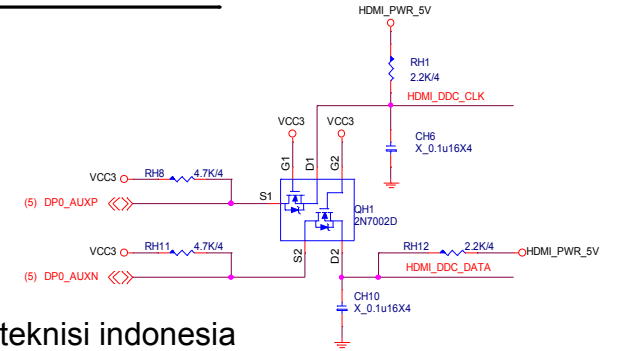
For HDMI 1.4



HDMI_MOS_DATA trace length <500mil
other platform please check design guide

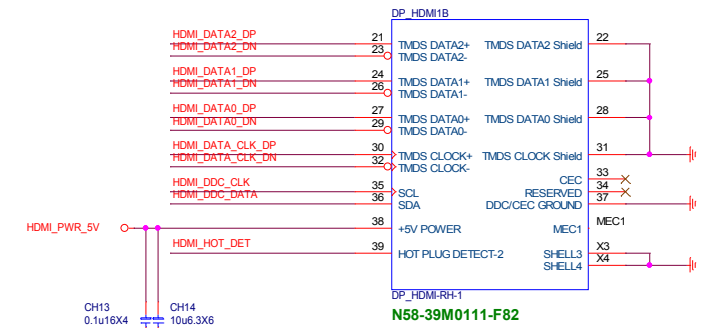


AUX Level Shifter

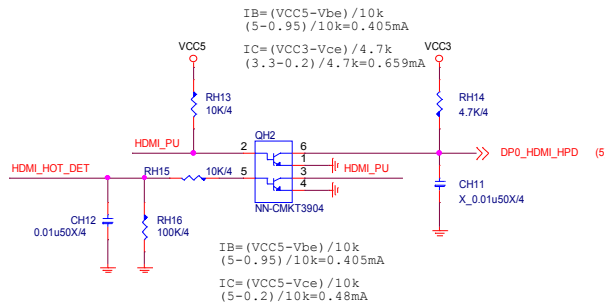


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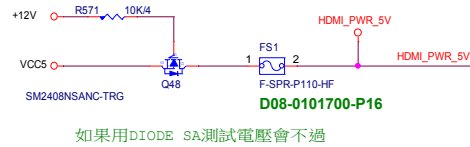
Connector



HPD Circuit

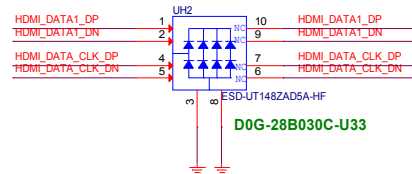
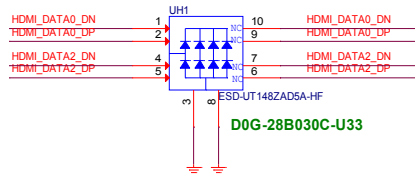


Connector Power

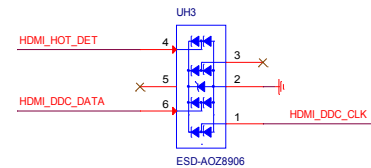


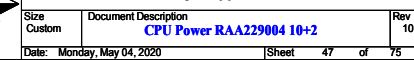
如果用DIODE SA测试电压会不过

For EMI

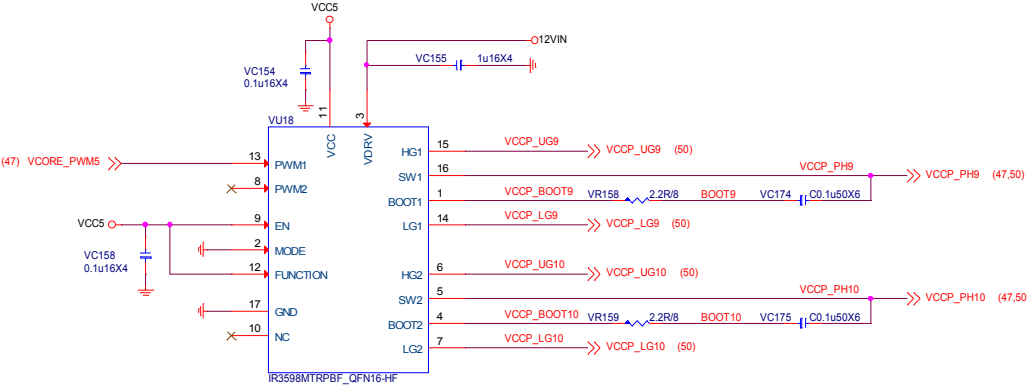
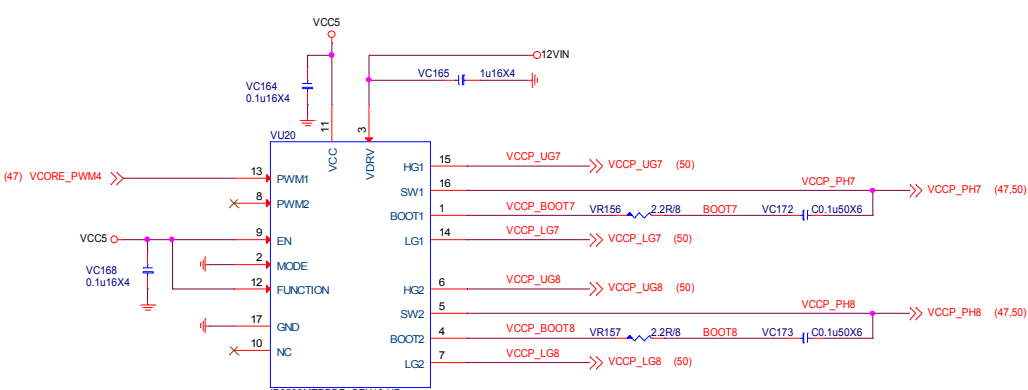
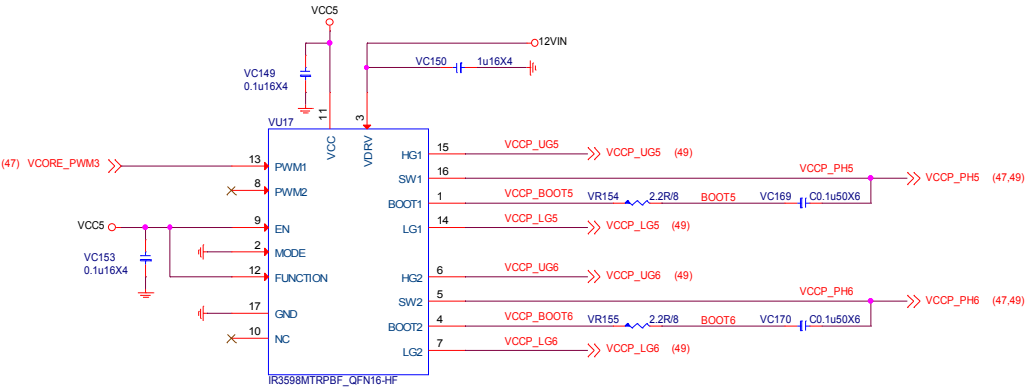
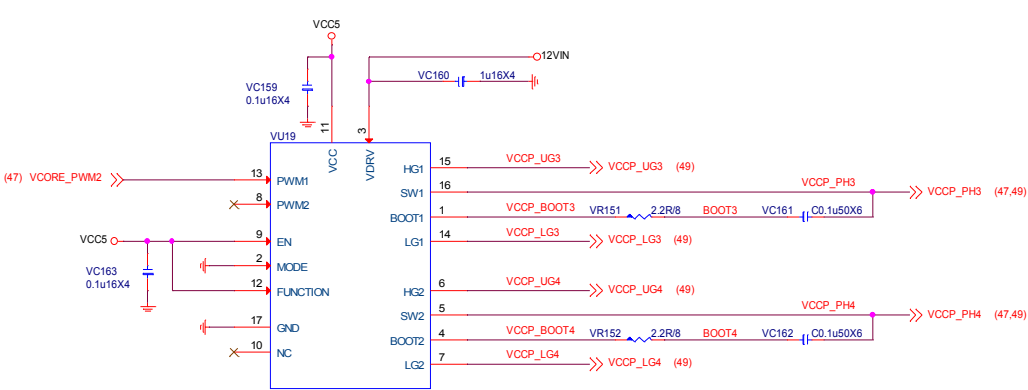
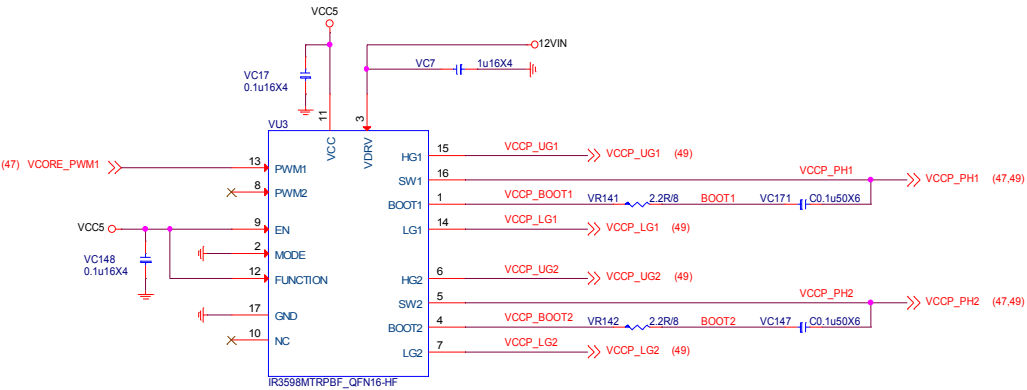


注意:耐壓5v零件

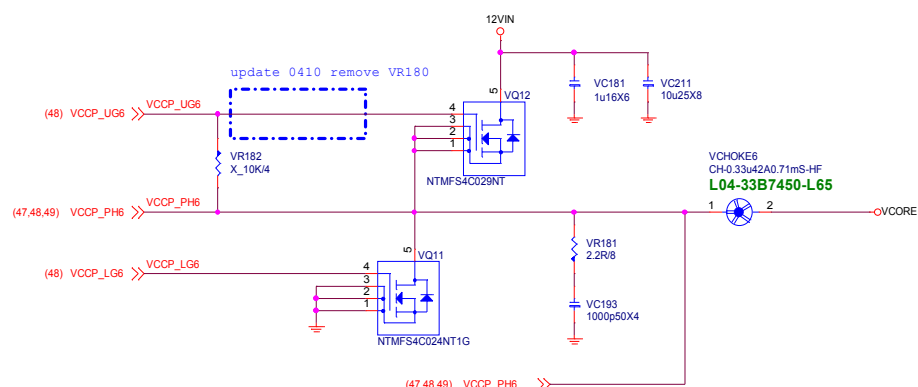
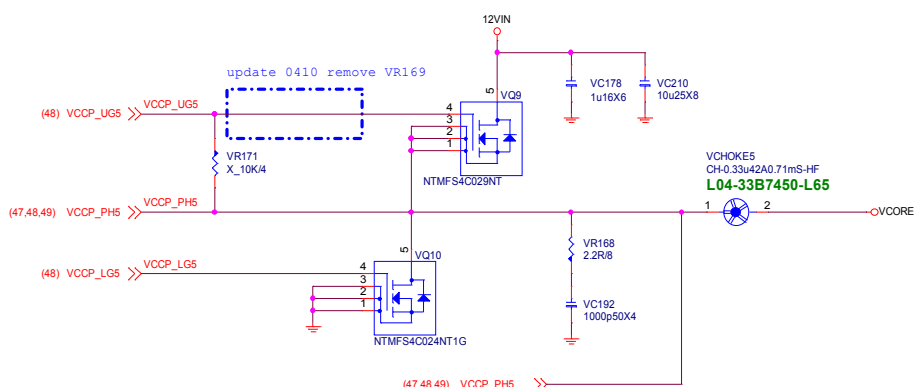
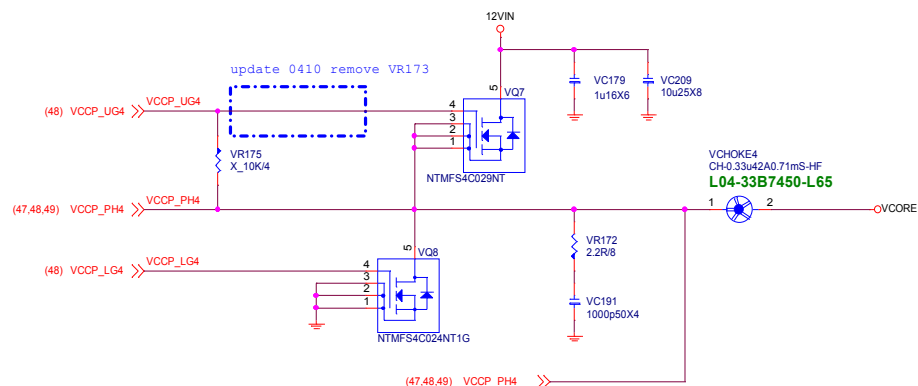
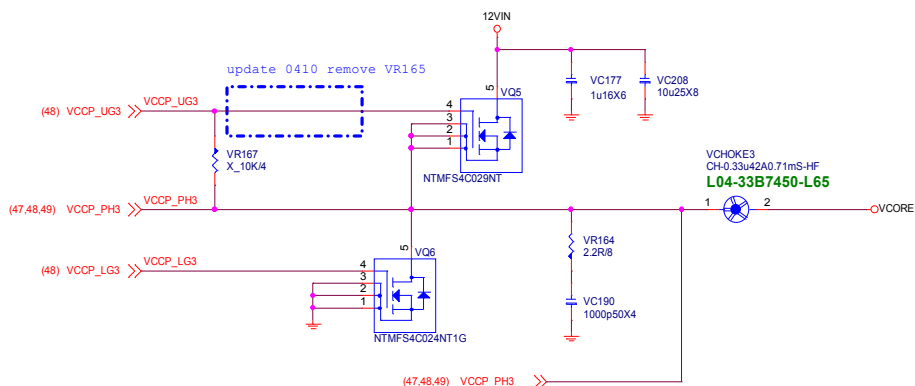
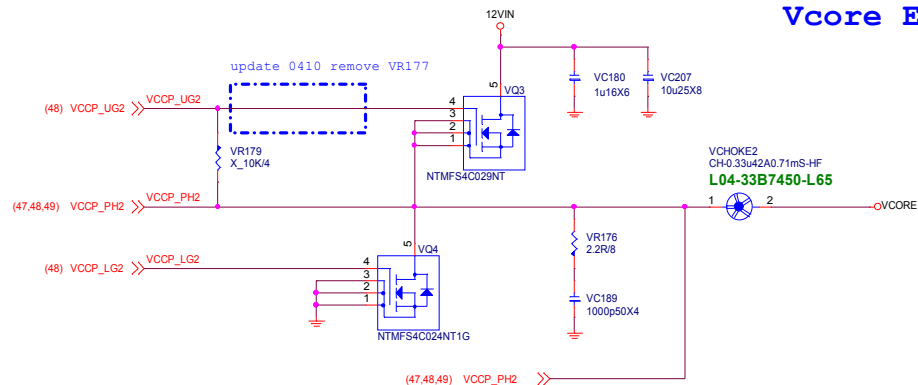
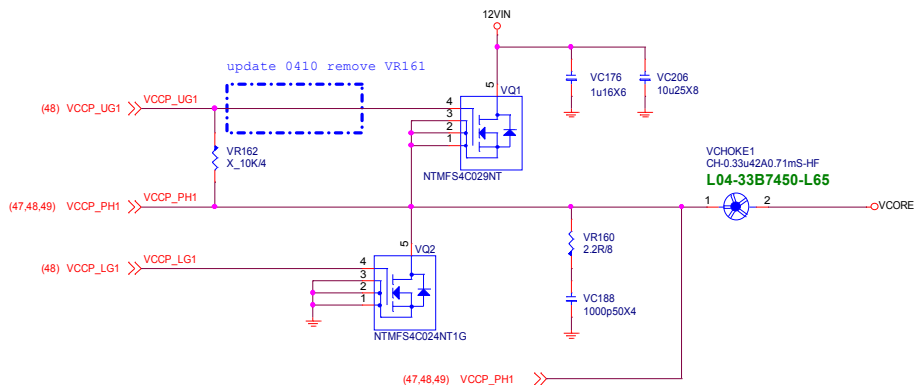




CPU_CORE Driver IC VCORE Double 10-PHASE



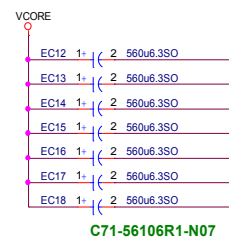
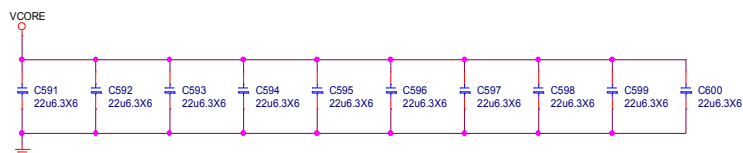
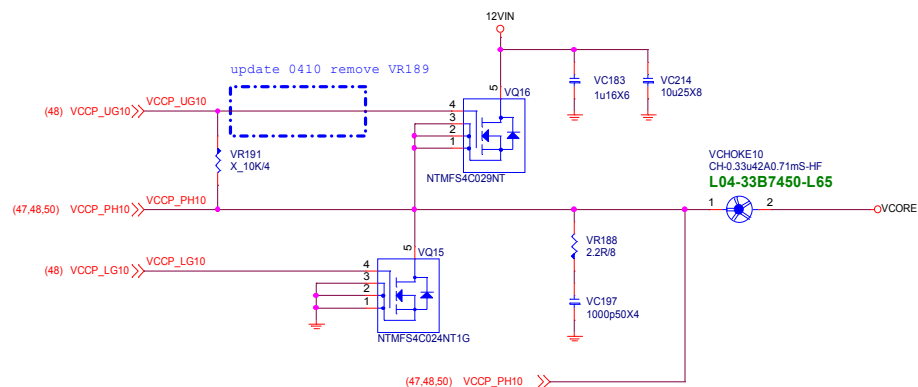
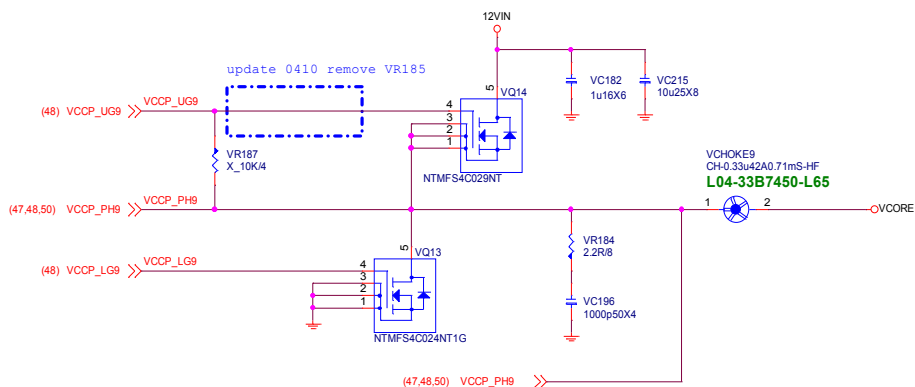
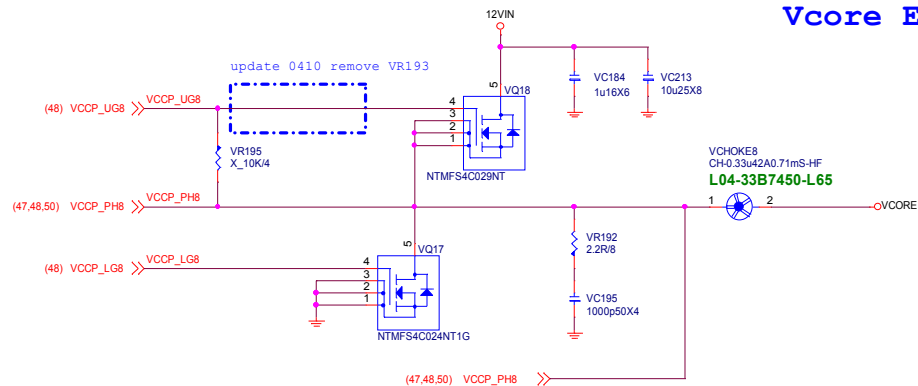
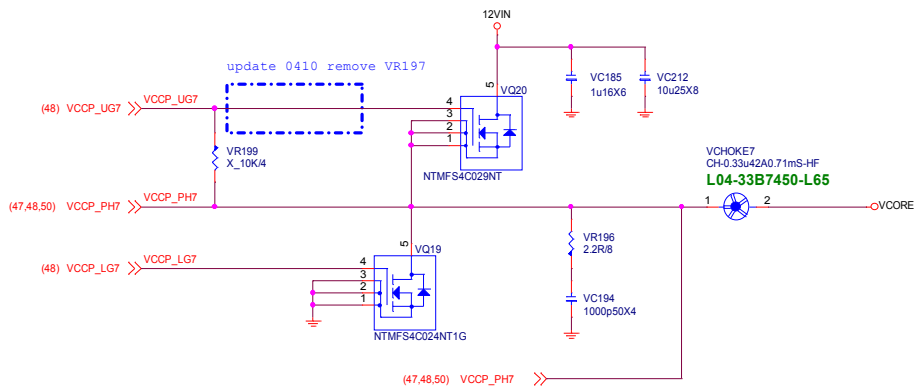
Vcore EDC Max 140A

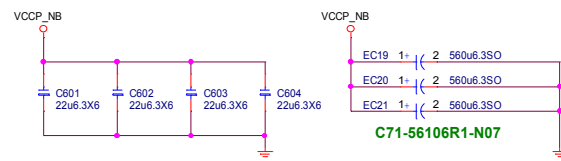
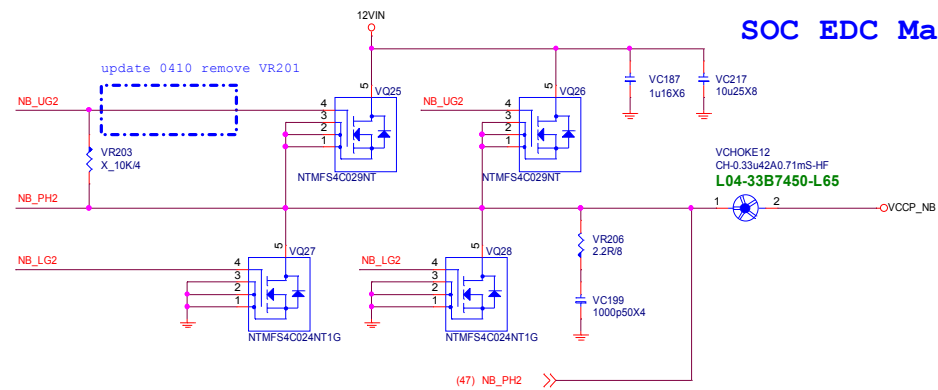
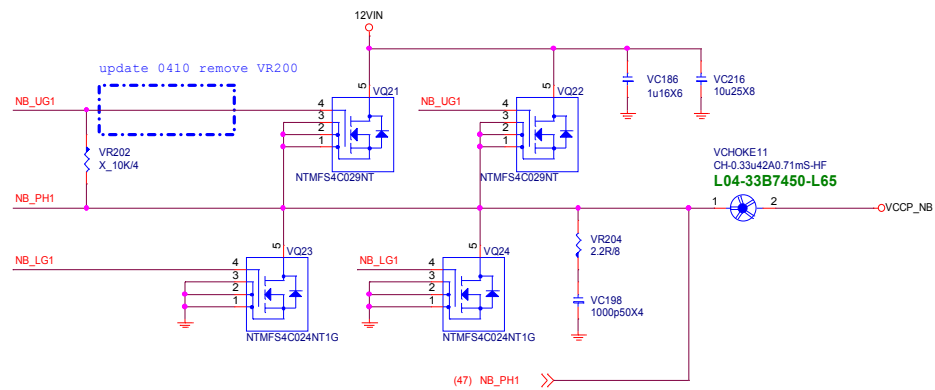
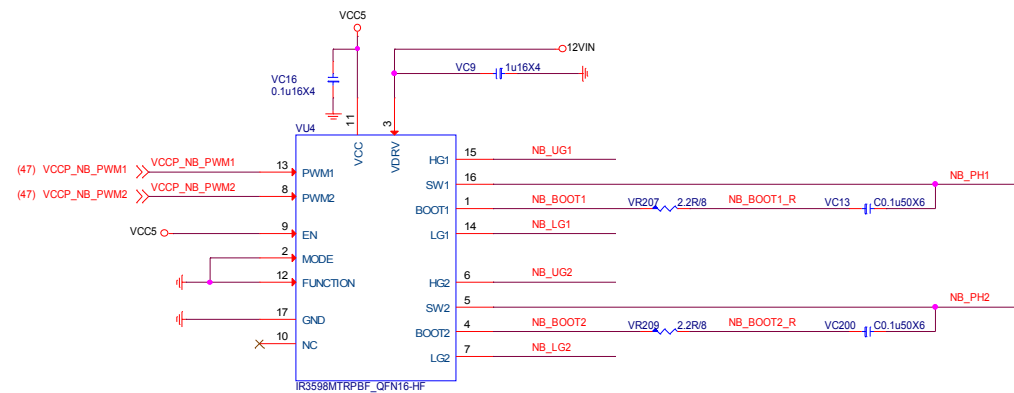


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Size	Document Description	Rev
Custom	CPU Power Vcore Phase 1-6	10
Date: Monday, May 04, 2020	Sheet 49 of 75	

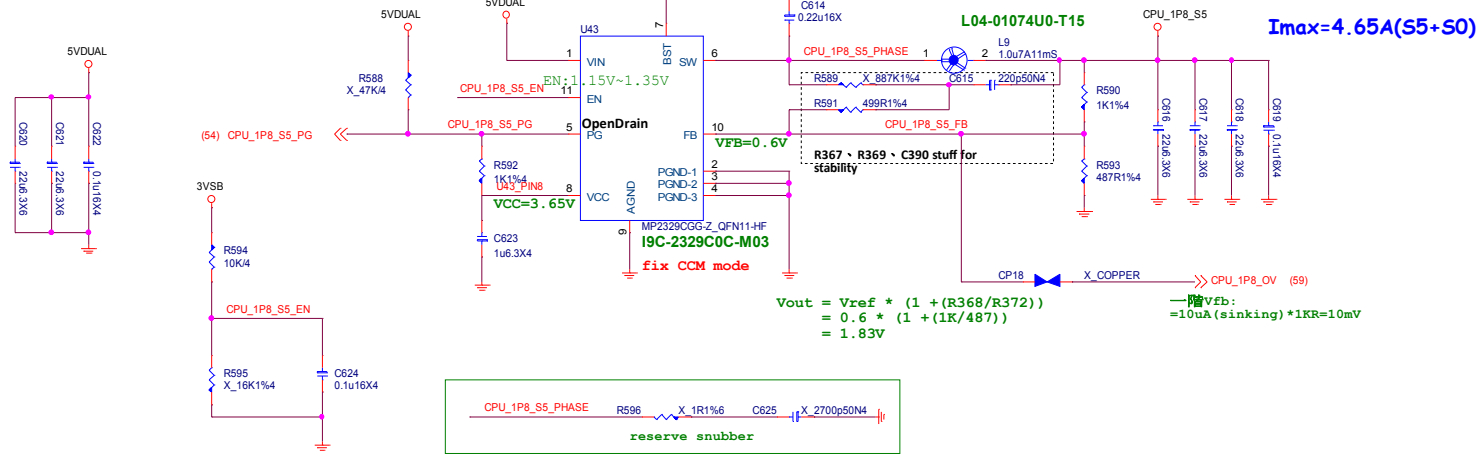




CPU 1.8V S5

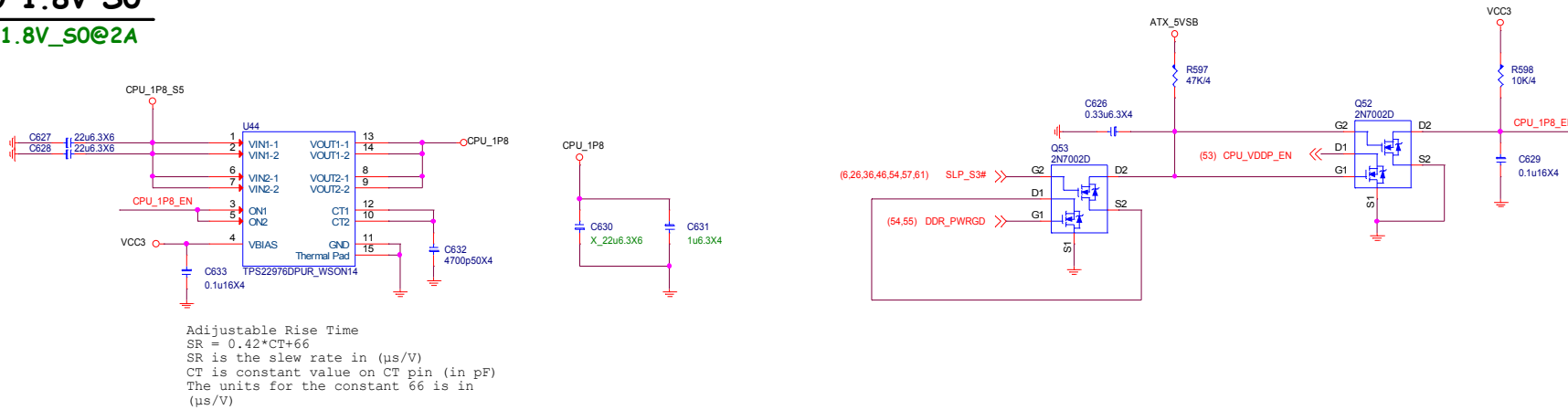
CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A
For VCCP_NB_S5 @0.9A

Input Current = $(6.5A \cdot 1.8V) / 5V / 0.8 = 3A$



CPU 1.8V S0

CPU 1.8V_S0@2A



DDR_PWRGD

CPU_VDDP

CPU_1P8

VDD33



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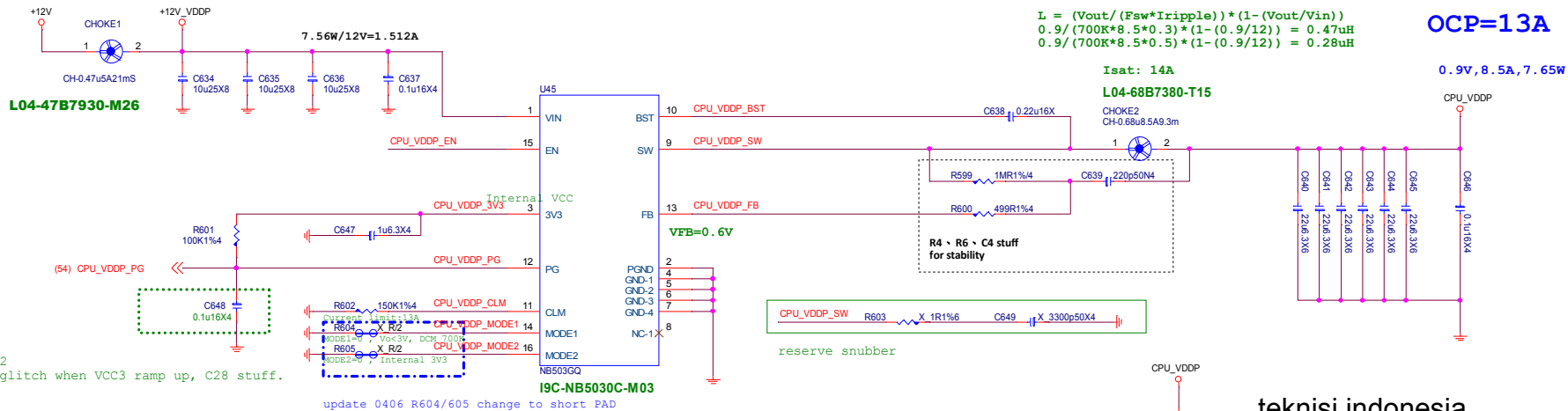
MS-7C56

Size	Document Description	Rev
Custom	CPU Power 1.8_S0 / S5	10
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CPU_VDDP_S0

0.9V@S0:8.5A

Input Current = $(13A \cdot 0.9V) / 12V / 0.8 = 1.22A$
 Choke Isat = 8A
 $I_{rms} = I_{out} \cdot \sqrt{D} \cdot \sqrt{(V_o/V_i) \cdot (1 - (V_o/V_i))}$
 $= 13 \cdot \sqrt{0.9/12} \cdot \sqrt{(1 - (0.9/12))} = 3.42A$
 Choke I_rms = 5A



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$$V_{out} = V_{ref} + (R1 \cdot R4 \cdot V_{ref}) / (R2 \cdot (R1 + R4))$$

$$= 0.6 + (1k \cdot 1000k \cdot 0.6) / (1.96k \cdot (1k + 1000k))$$

$$= 0.9058V$$

TYPE0_CPU_SEL
 0: RV/RR
 1: BR/SR/PR/MTS/VR

TYPE0_CPU_SEL:
 0: TYPE 2
 1: TYPE 0

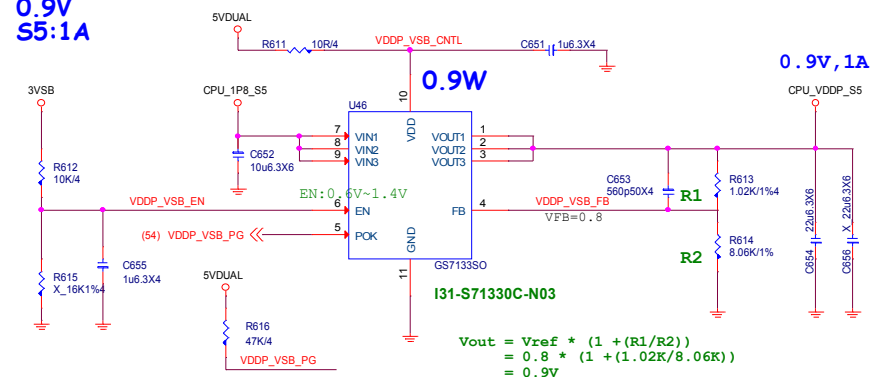
CPU_VDDP_EN:
 X: BR/SR/PR/MTS/VR
 O: RV/RR

CPU_VDDP_EN:
 X: BR/SR/PR/MTS/VR
 O: RV/RR

CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SR/RR
NA	0	0	0	0
SR	2	1	0	CPU VDDP NOT SUPPORT TYPE2
RV/RR	3/5	0	1	1
MTS/VR	4/6	1	0	CPU VDDP NOT SUPPORT TYPE4/6

CPU_VDDP_S5

0.9V
 S5:1A



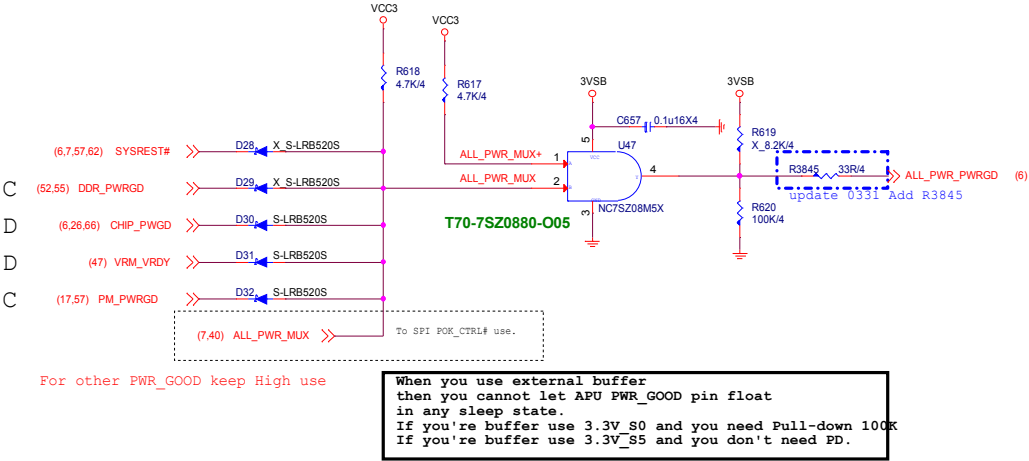
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MS-7C56

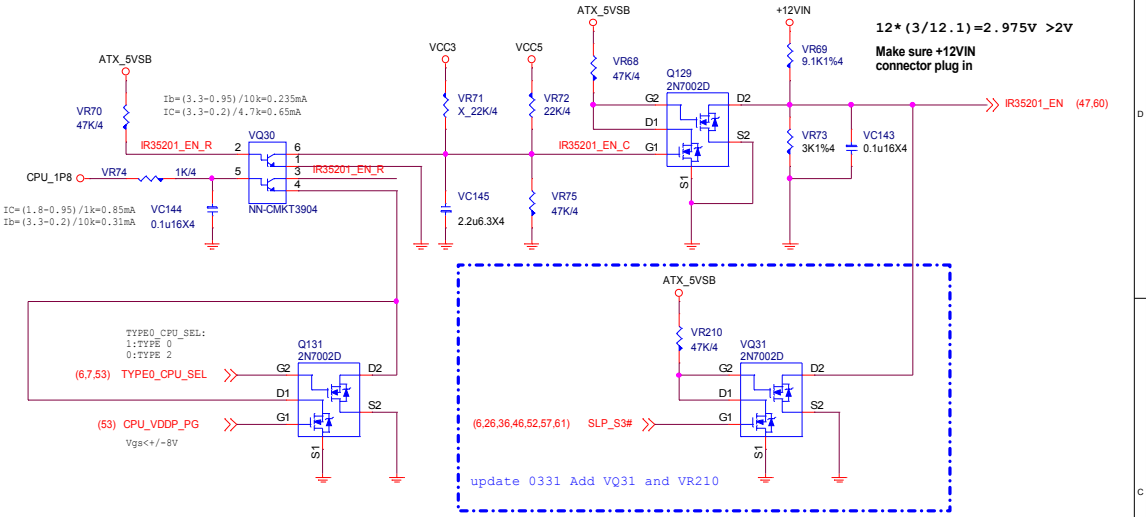
Size	Document Description	Rev
Custom	CPU Power VDDP - NB503	10
Date:	Monday, May 04, 2020	Sheet 53 of 75

ALL POWER GOOD MUX

S0 PG

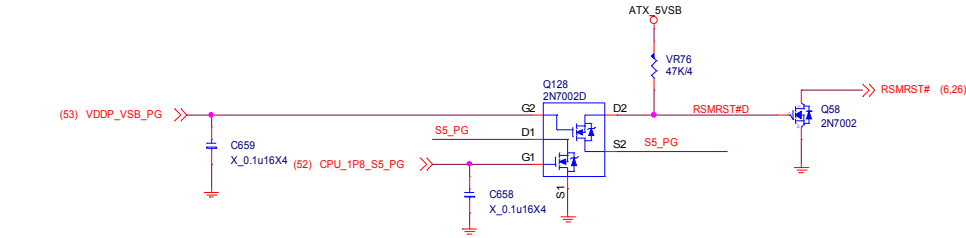


VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA	1	0	0
SR	2	1	0
RV/ZP	3	1	0
MTS	4	1	0

S5 PG



DDR4_1.2V@28.7A

18A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

Rocset=1.5*Imax*Rdson(Low side)/Iocset
=1.5*28.7A*2mohm/10uA
=8.61K

OCP = 35A; Choke Isat=50A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R639 = 35 * 2mohm / 10uA
R639 = 7K

Rdson(Low Side) 5V

D03-4C02403-005:3.3 ~ 4mohm

DDR_VR_EN
FROM SIO_VDDQ_EN:R230/R220 stuff
FROM VPP_VR_PG:R230/R220 un stuff

Default:FCCM
4.5V:FCCM
2.37V:DEM

update 0327 remove VPP_VR_PG
0423 R633 change to short PAD

update 0327 remove Q64 and R640

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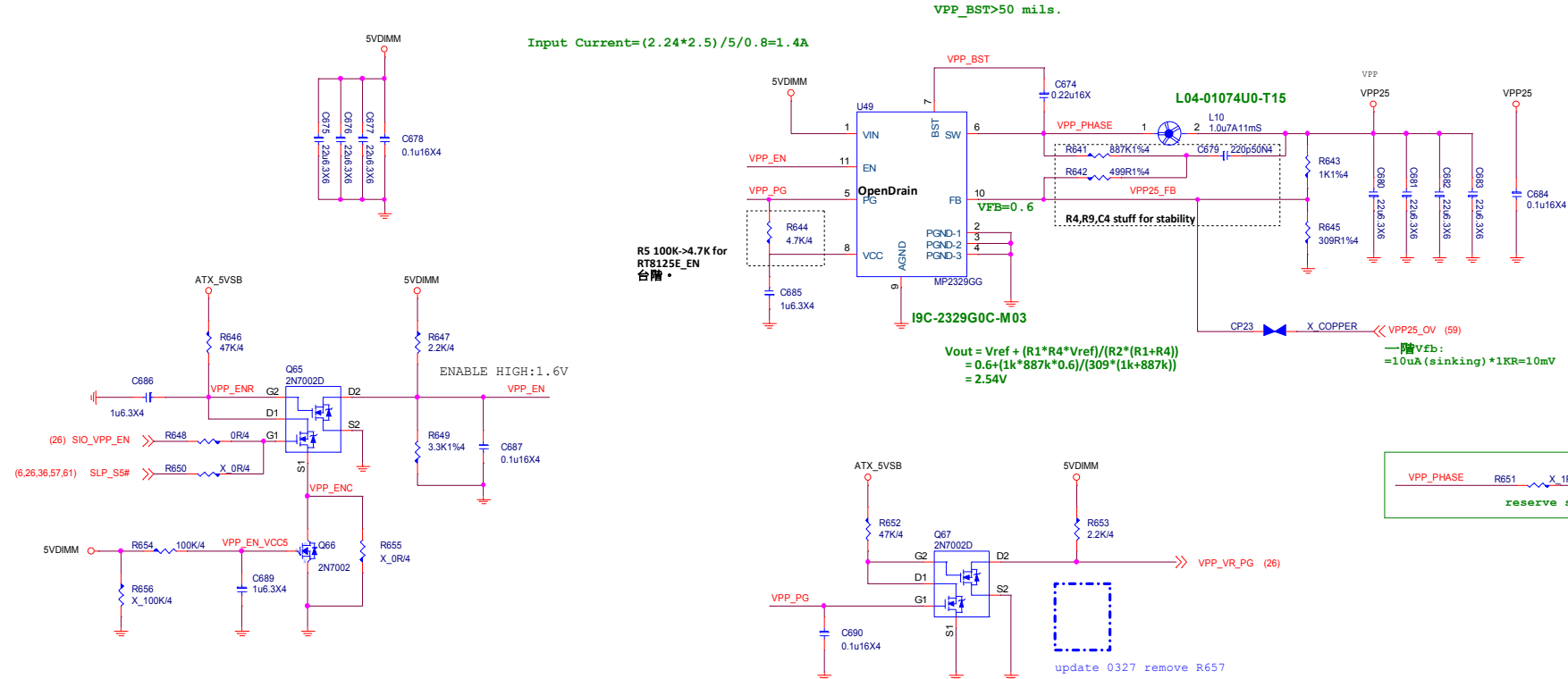
Input Current=(28.7*1.2)/5/0.8=8.61A

Rocset=1.5*Imax*Rdson(Low side)/Iocset
=35A*2mohm/10uA
=7K

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MS-7C56			
Size Custom	Document Description DDR Power - 8125H		Rev 10
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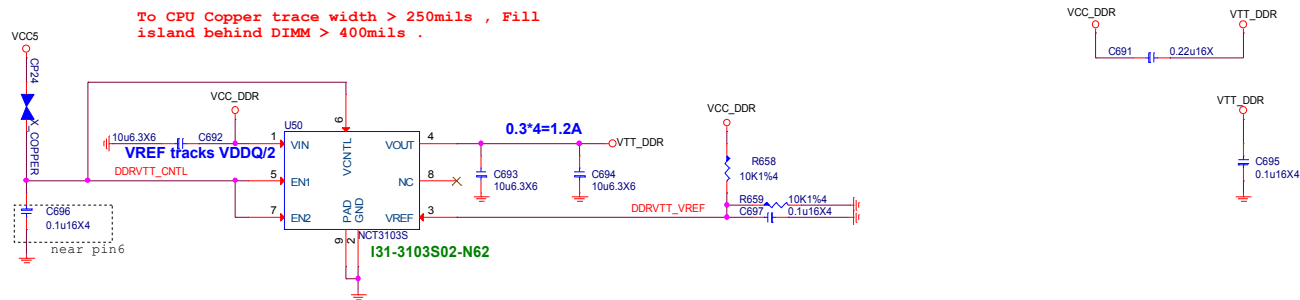
4DIMM : VPP25

2.5V@2.24A



DDR VTT Power

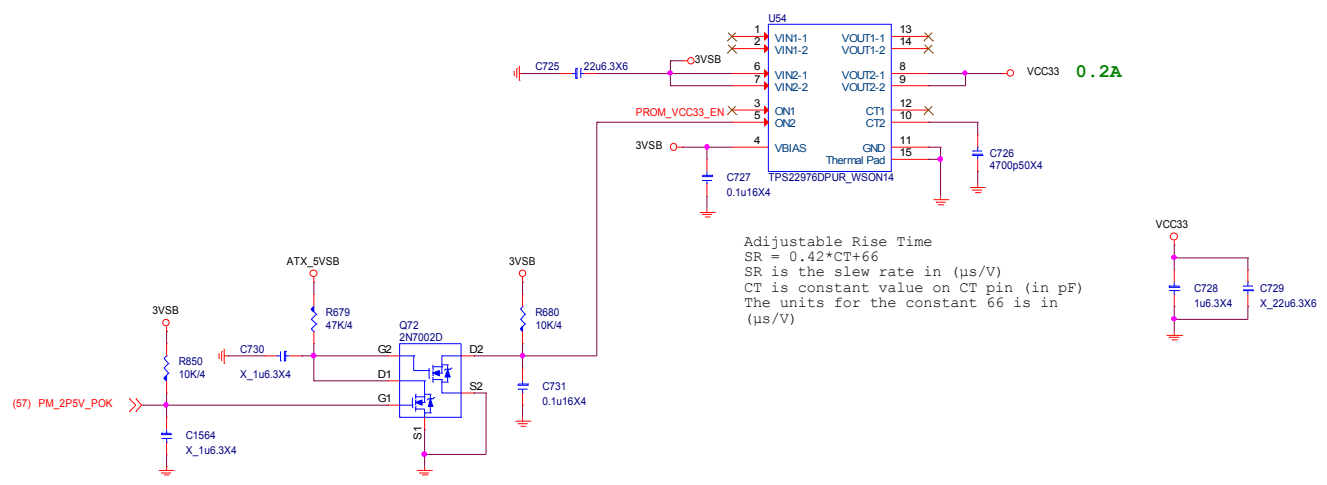
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



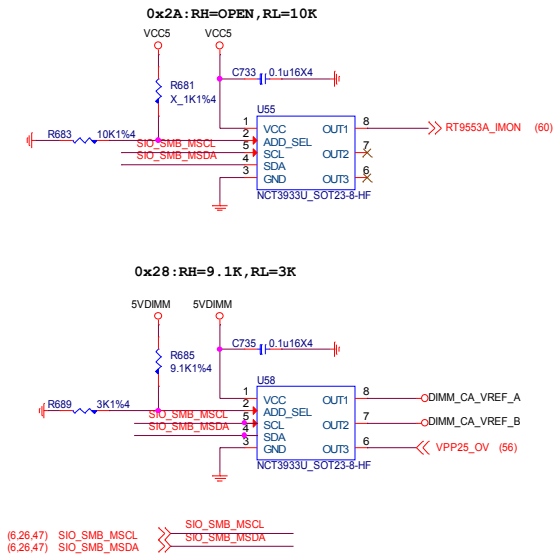
Size Custom	Document Description PM - SY8288/PM_1P05/PM_2P5V	Rev 10
Date: Monday, May 04, 2020	Sheet 57 of 75	

PROM VCC33

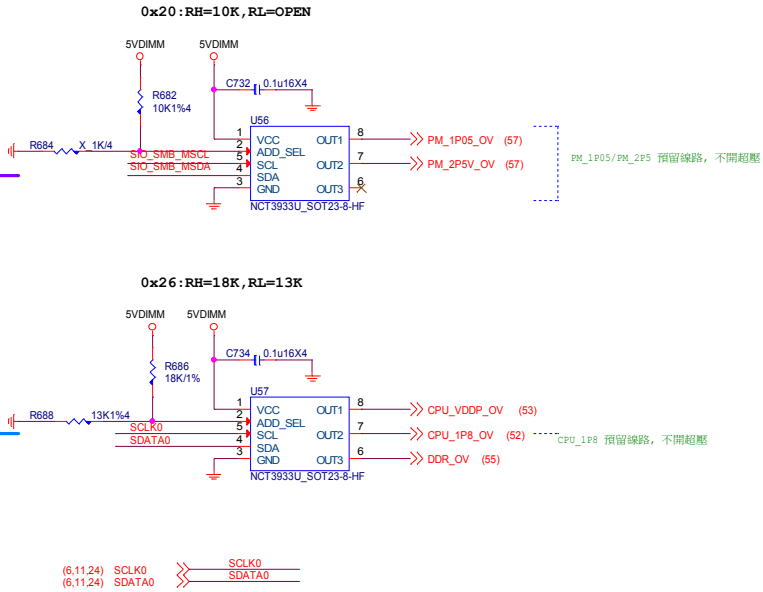
VCC33@0.2A



Over Voltage Control IC

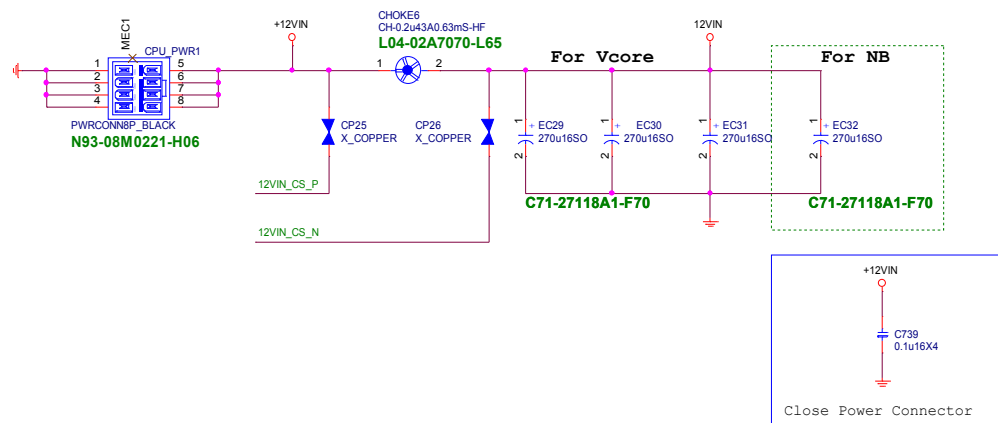


UPI VOLTAGE CONSOLE					
ADDRESS	0x2A	0x28	0x26	0x24	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3
RL (KOhm)	10	1.3	2.3	3	3.9
BUS_SEL	0%	25%	40%	60%	75%
					100%



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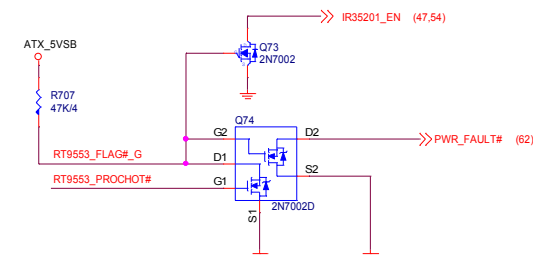
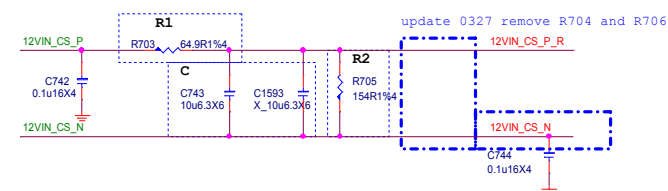
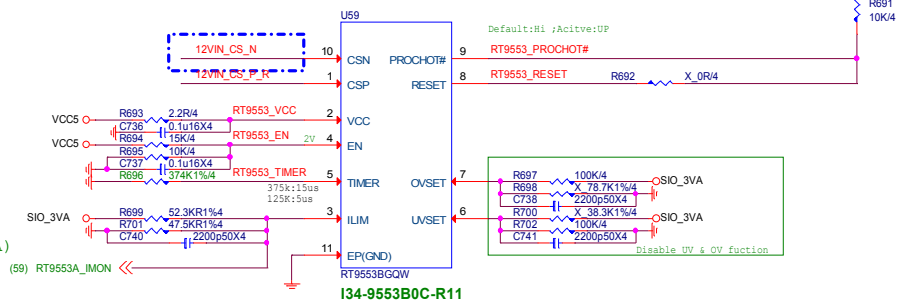
CPU POWER CONNECTOR



$$\Delta V_{ILIM} = 10\mu A * [(60.4K * 40.2K) / (60.4K + 40.2K)] = 226mV$$

$$I_{sense} = V_{ILIM} / 100 * R_{sense}$$

$$\Delta I_{sense} = 226\text{mV} / 100 * 0.39\text{m} = 5.795\text{A}$$



Vcore	D=Vout/Vin		SOC	D=Vout/Vin	
Vin = 12	> input voltage		Vin = 12	> input voltage	
Vout = 2	> output Vcore		Vout = 1.55	> output Vcore	
D = 0.166667			D = 0.129167		
I o = Icore(max)*0.8			I o = Icore(max)*0.8		
I core(max) = 200	> Vcore current		I core(max) = 75	> Vcore current	
I avg. = 160	A		I avg. = 60	A	
I ripple={ I o*√ D*√ (1-D)} / Phase			I ripple={ I o*√ D*√ (1-D)} / Phase		
Phase = 10	phase		Phase = 2	phase	
I ripple = 5.962848	A		I ripple = 10.06153	A	
How many pcs. Of Cap.			How many pcs. Of Cap.		
I ripple(cap) = 4700	m A		I ripple(cap) = 4700	m A	
COE _{TEMP} = 1			COE _{TEMP} = 1		
Input Cap. = 2	pcs.		Input Cap. = 3	pcs.	

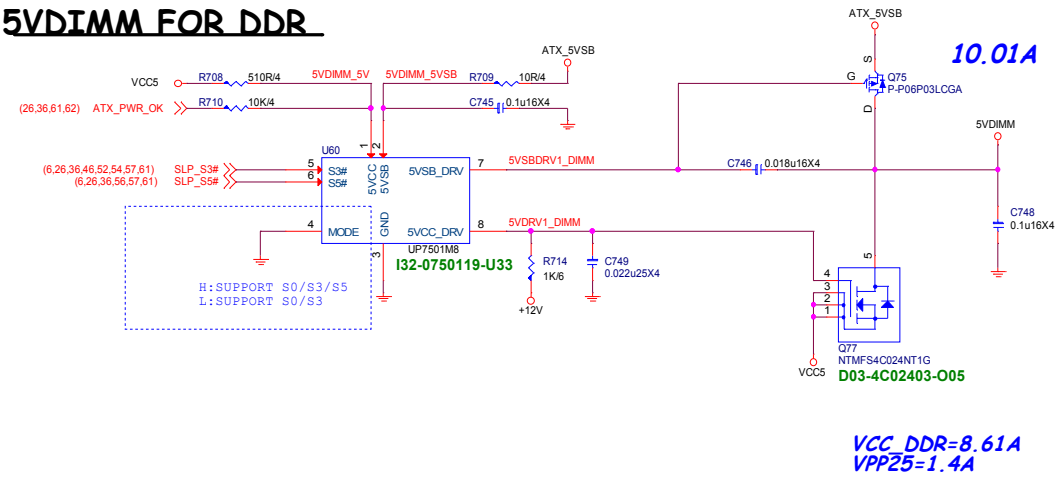


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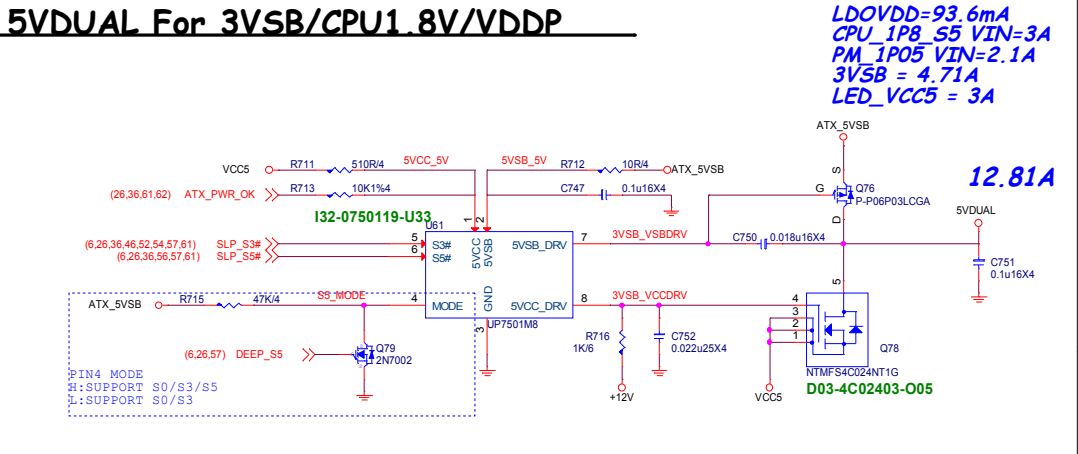
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Size Custom	Document Description OCF 12VIN - RT9533B	Rev 10
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5VDIMM FOR DDR



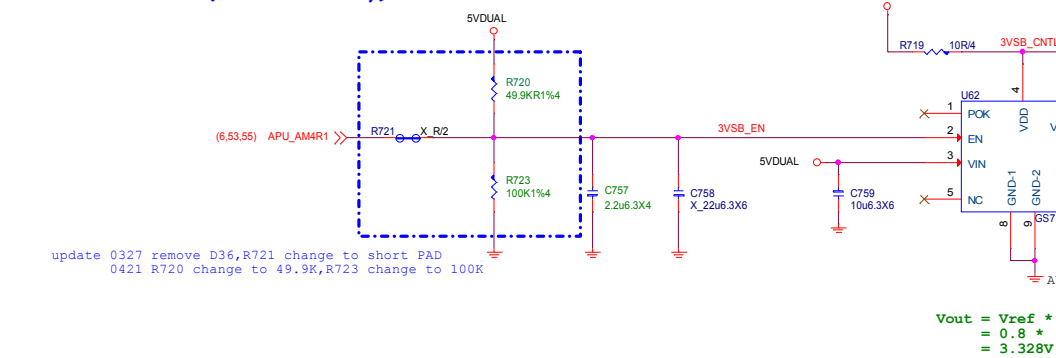
5VDUAL For 3VSB/CPU1.8V/VDDP



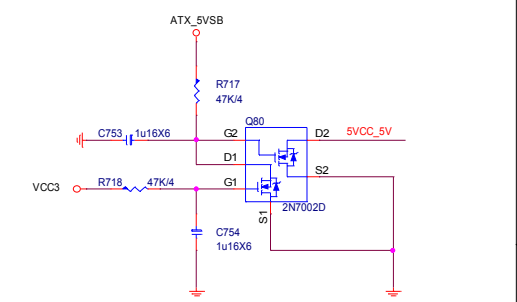
3VSB cost down

3.3V@4.305A

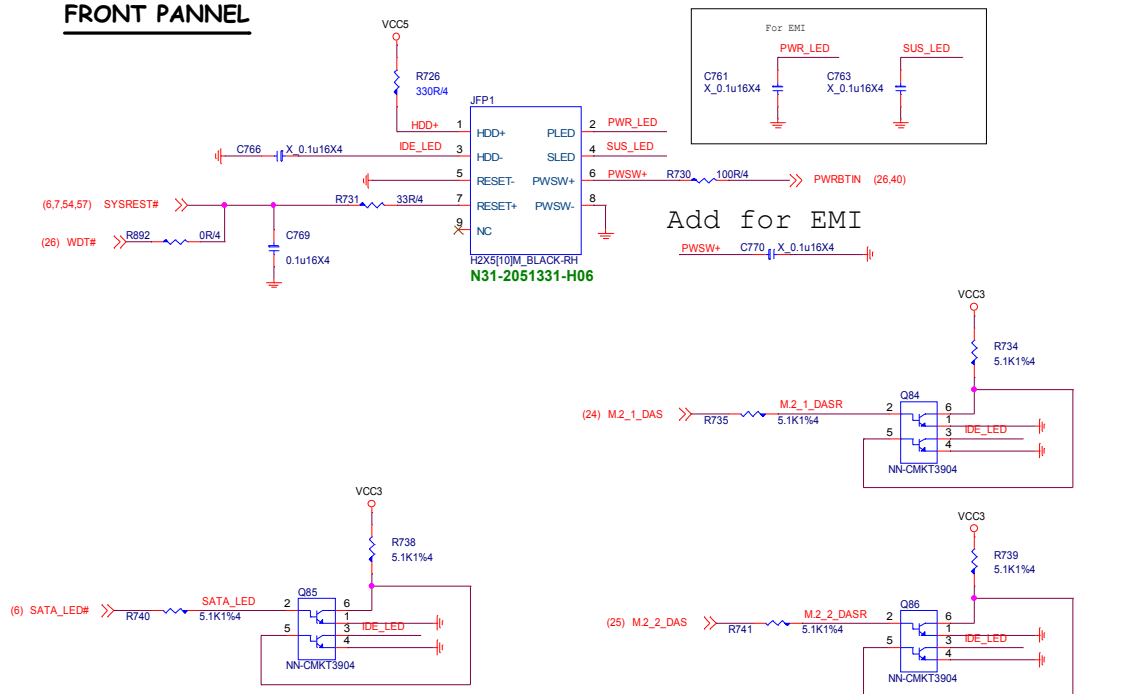
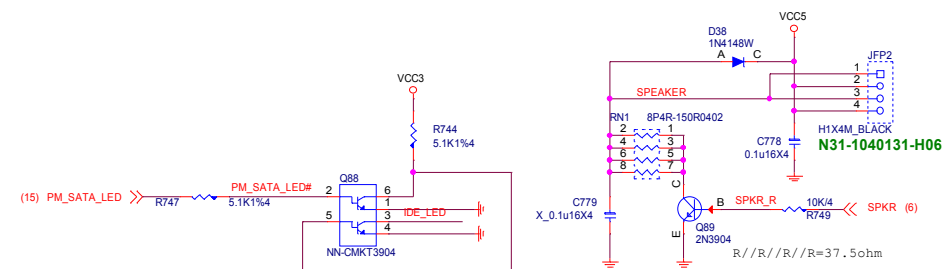
CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIe=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
PCH VCC33 :0.2A(Modern Standby)



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



FRONT PANNEL

[illegible]

MS-7C56

Size Custom	Document Description ATX power - FrontPanel / EMI	Rev 10
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EZ Debug LED

The diagram illustrates the EZ Debug LED system, which uses four LEDs to indicate the status of different components: CPU, DRAM, VGA, and DEVICE. Each LED is controlled by a specific GPIO pin through a transistor and resistor network.

LED States Table:

LED GPIO	GPIO44	EGPIO96	GPIO45	GPIO47
亮 (ON)	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅 (OFF)	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

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LEDGPIO	GPIO44	EGPIO96	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

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LED_SW1 **FORM SIO**

D0C-040P100-H91/D0C-040S500-E07

LED SW1 for ALL LED OFF

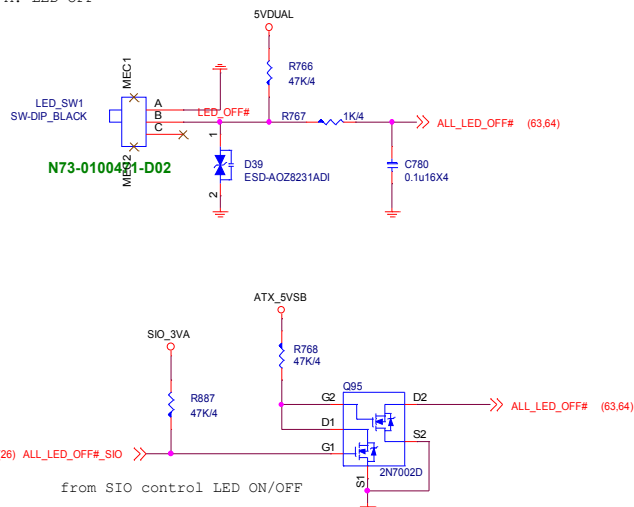
B-C: LED ON(default)
B-A: LED OFF

The diagram illustrates the internal structure of the LED_SW1 (SW-DIP_BLACK) and its connection to the ALL_LED_OFF# signal. The switch has three pins: A, B, and C. Pin A is connected to the 5VDUAL supply through a 47K resistor (R766). Pin B is connected to the LED_OFF# signal. Pin C is connected to the LED_OFF# signal through a 1K resistor (R767). The LED_OFF# signal is also connected to the ALL_LED_OFF# signal (63,64) through a 1K resistor (R767). A diode (D39, ESD-AOZ8231ADI) is connected between the LED_OFF# signal and the ALL_LED_OFF# signal. A capacitor (C780, 0.1u16X4) is connected between the ALL_LED_OFF# signal and ground.

The diagram also shows the connection of the LED_SW1 to the SIO control LED ON/OFF signal. The SIO_3VA supply is connected to the LED_SW1 through a 47K resistor (R887). The ATX_5VSB supply is connected to the LED_SW1 through a 47K resistor (R768). The LED_SW1 is connected to the ALL_LED_OFF# signal (63,64) through a MOSFET (Q95, 2N7002D) and a diode (D2). The MOSFET is controlled by the SIO control LED ON/OFF signal through a gate resistor (G1, 2N7002D). The MOSFET is also connected to the ALL_LED_OFF# signal (63,64) through a drain resistor (G2, 2N7002D).

LED SW1 for ALL LED OFF

```
B-C: LED ON (default)
B-A: LED OFF
```



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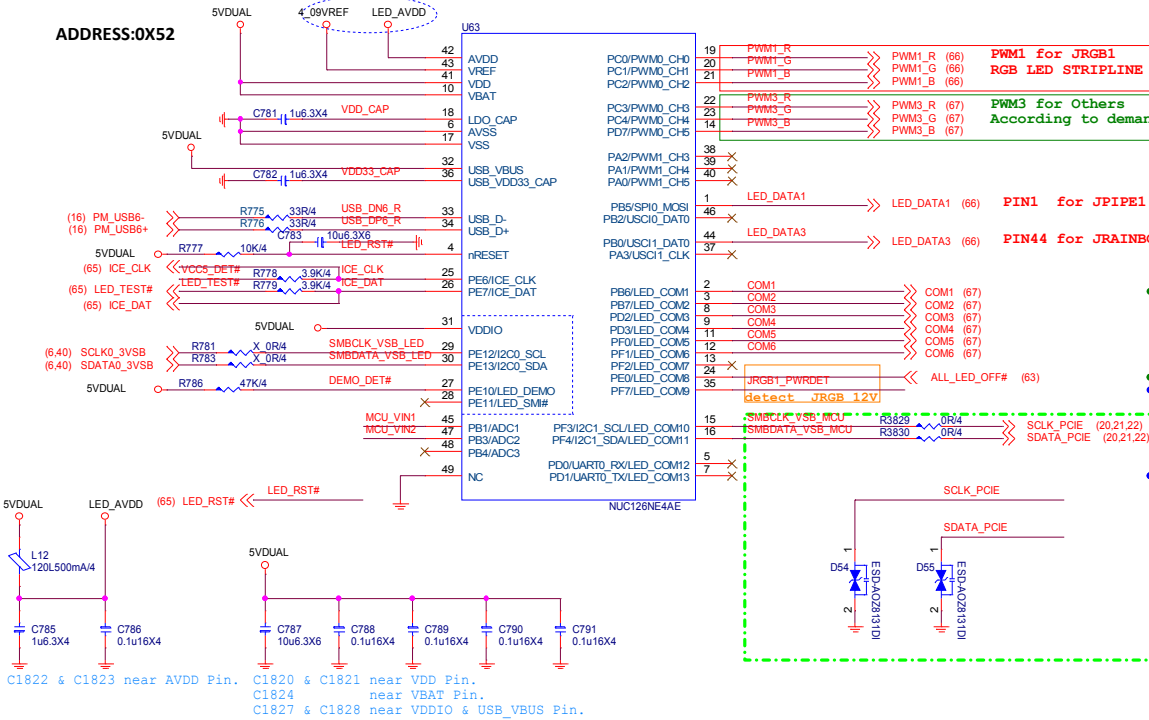
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Size Custom	Document Description LED - EZ DEBUG / AMP	Rev 10
Date: Monday, May 04, 2020		Sheet 63 of 75

48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

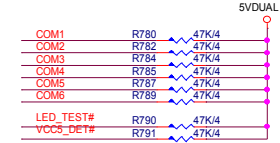
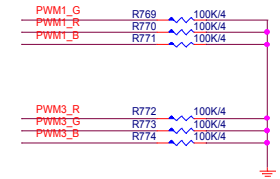


COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.

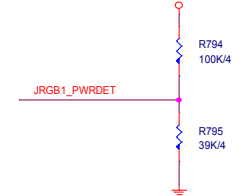
COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized
onboard LED control.

PS. COM1 is the first action block,
next is COM2, and so on.

Pin15,16 can configure to master
smbus if spec requirement.



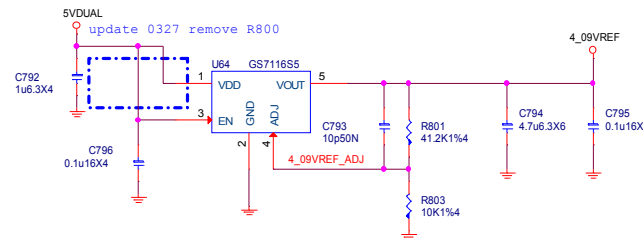
detect JRGB 12V



Clear MCU Circuit



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2



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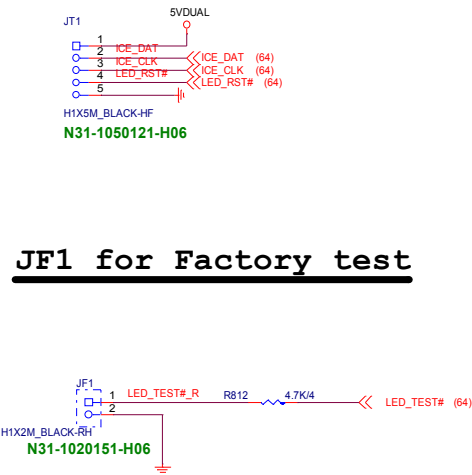
EXTERNAL POWER INPUT

External Power

1 PCH HEATSINK LED

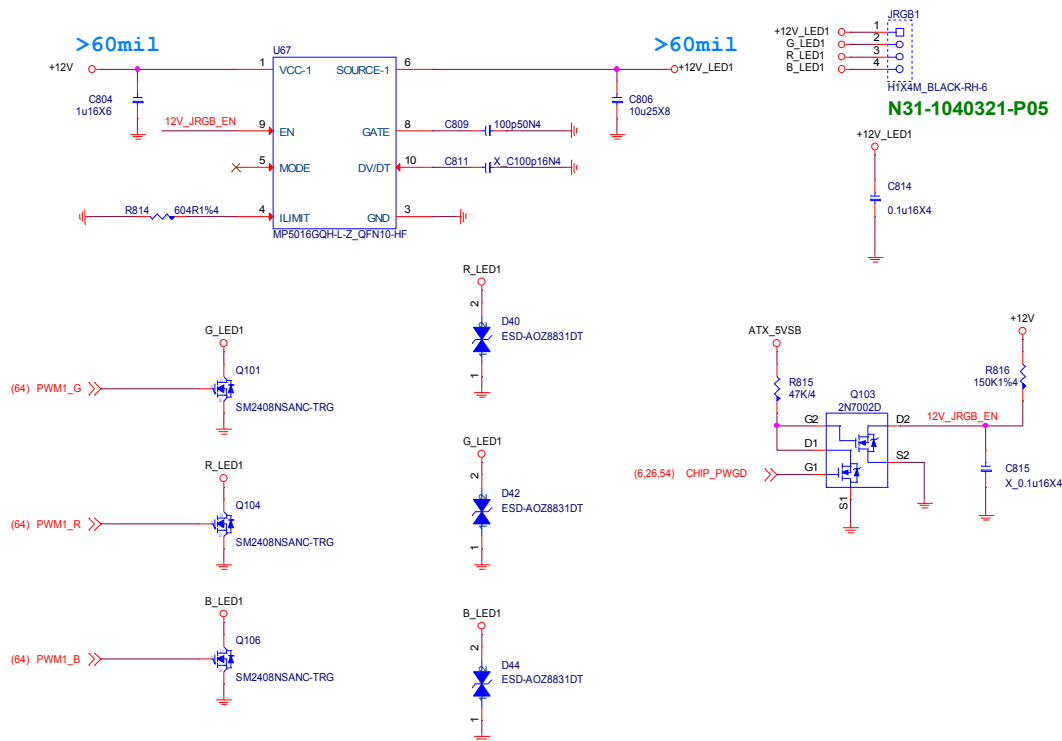
For MOS

JT1 for FW update

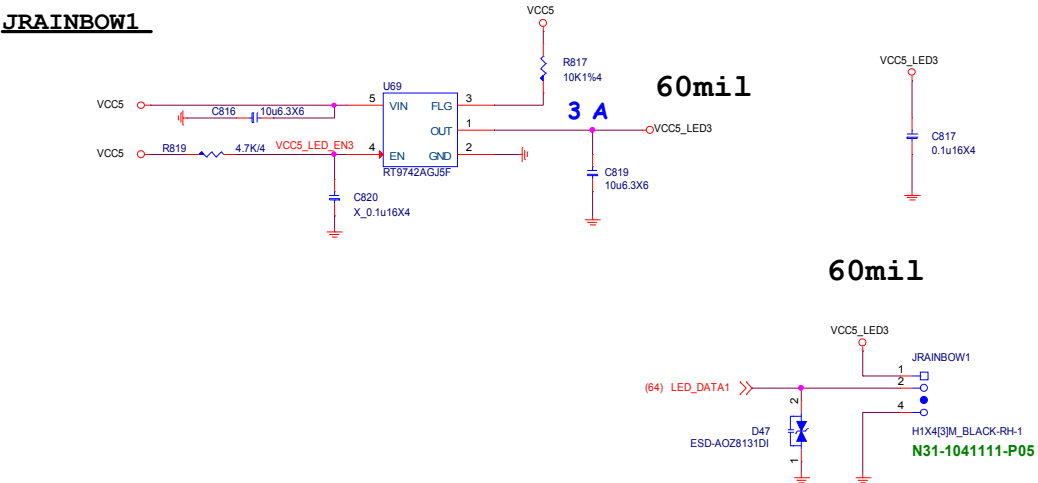
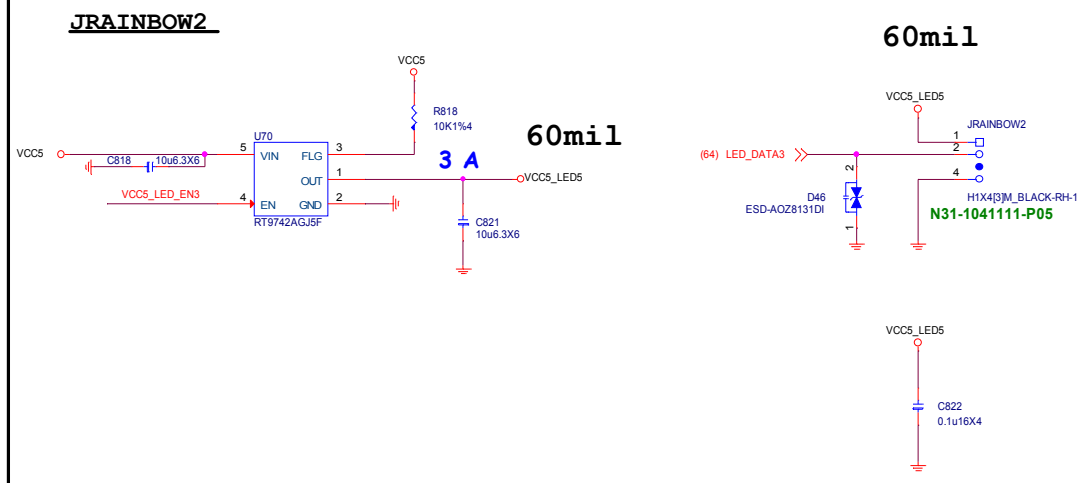


JF1 for Factory test



JRGB1JRGB2

JRAINBOW1

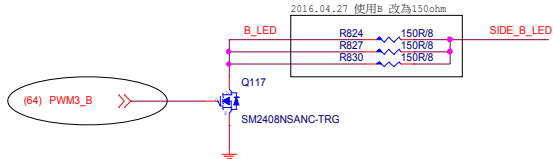
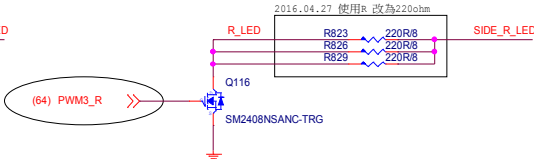
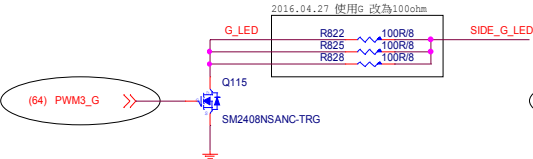
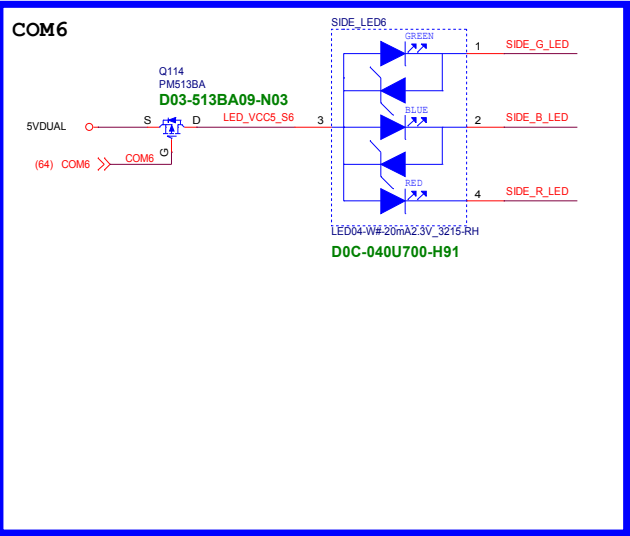
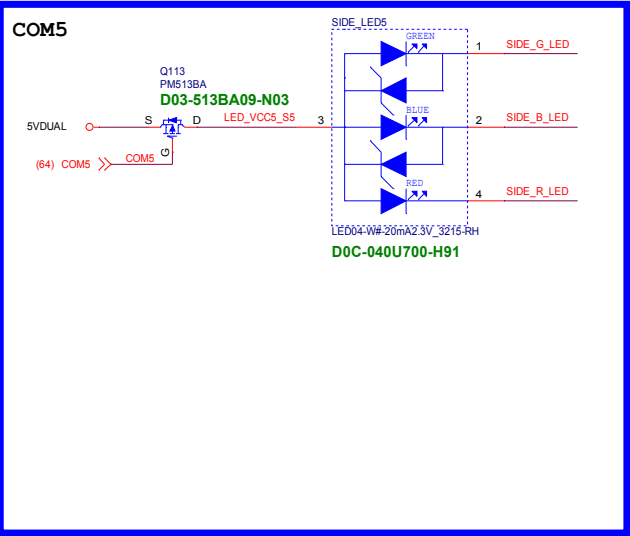
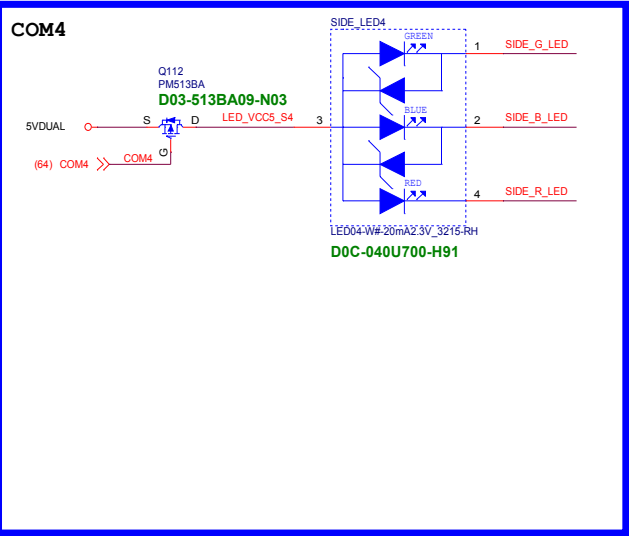
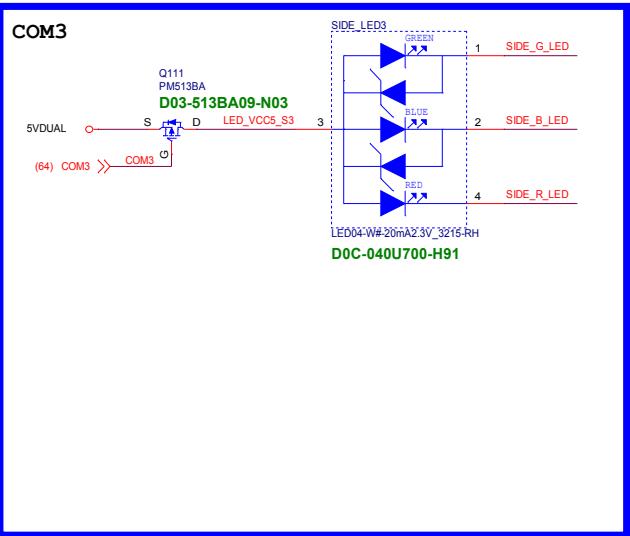
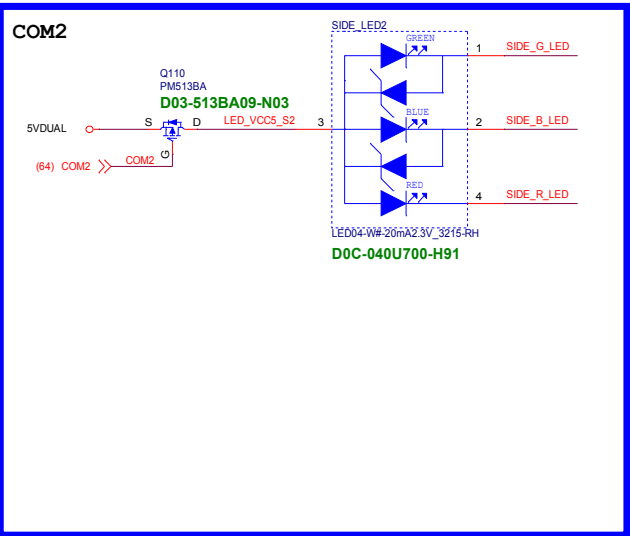
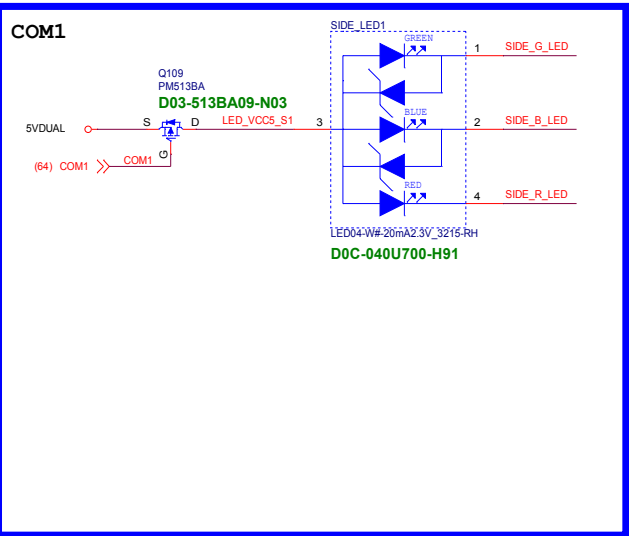
JRAINBOW2

MICRO-STAR INT'L CO.,LTD

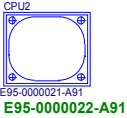
MS-7C56

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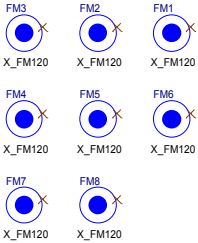
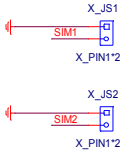
BOARD SIDE LED *6



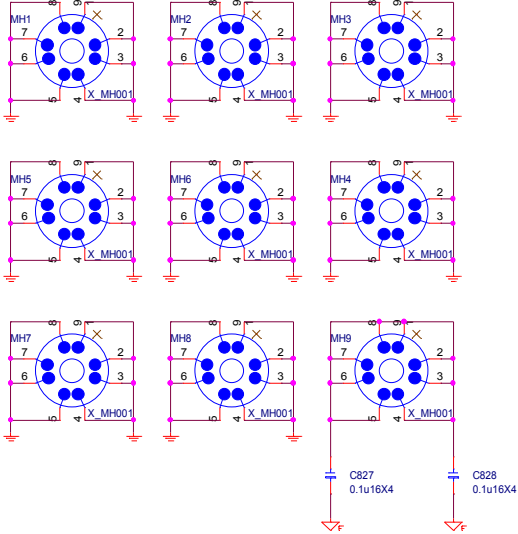
CPU Socket



Simulation



Optics Orientation Holes



MANUAL PART

AMI_LAB1
G51-M1SPXXA-A09
G51-M1SPXXA-A09

CFOS1
X_Y02-MU00170-CFO
Y02-MU00170-CFO

HDMI_LA1
HDMI1
HDMI LABEL
Y01-RHDMI03-000

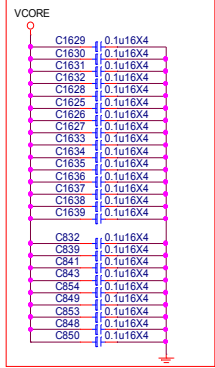
MKT_LA1
MKT LABEL
X_MKT LABEL
G51-M1SPP78-Q13

NAHIMIC_LA1
NAHIMIC
X_NAHIMIC_LA1
Y02-MU00100-NAH

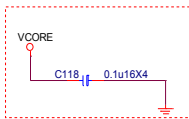
BAT1_X1
BAT-BCR2032P
AVL1
D06-0100161-F52
D06-0100101-K26

Moat CAP

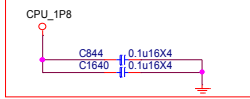
For cross moat



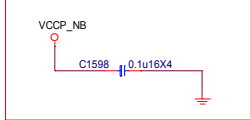
add for cross moat



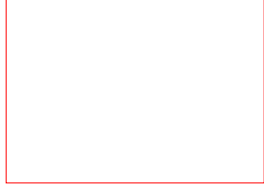
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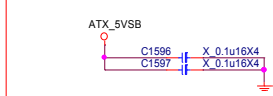
For SVID cross moat



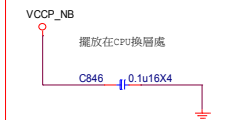
For cross moat



Reserve for bypass 12VIN noise use



For cross moat



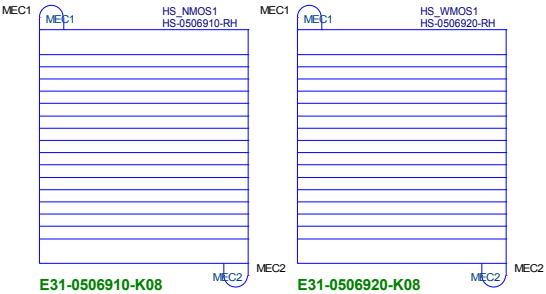
PCB

PCB



PD0-07C5610-E48, 昱鑫 (競華) 蘇州, 23, 微星 寶安恩斯通廠 (MSIS) 4, black
PD0-07C5610-G37, 精成-深圳, 57, 微星 寶安恩斯通廠 (MSIS) 4, black

MOS HEATSINK



PCH HEATSINK



IO cover



M2 HEATSINK

